Paper

Common-Mode Voltage Injection Techniques for Quasi-Two-Level PWM-Operated Modular Multilevel Converters

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This paper studies the application of common-mode voltage injection techniques typically used in two-level inverters (carrier-based space-vector modulation and flat-top modulation in particular) to quasi-two-level PWM-operated modular multilevel converters. Similar to two-level inverters, the available operating area is extended to higher modulation indices. The properties of the respective techniques are compared to each other and to the modular multilevel converter in the normal operation mode. The results are based on simulations and the model is partly experimentally validated on a downscaled converter prototype.

Keywords: modular multilevel converter, quasi-two-level, PWM, capacitance reduction

1. Introduction

The modular multilevel converter [1] (MMC, Fig. 1) is a well-known topology used in HVDC and medium-voltage applications. Recently, many efforts have been made to apply this topology to electric drives, as the low output frequencies would lead to an excessively high module capacitance in normal operation mode.

The majority of the proposed solutions can be divided into two groups. In the first group, the converter topology is modified, adding new current paths [2][3] or converter stages [4]–[6]. In the second group, an additional high-frequency voltage component is injected to the common-mode voltage [7]–[10]. While the first group increases the converter losses and the installed volume of semiconductor devices, the second group leads to converter oversizing, when the rated torque is demanded over the whole operating range [10]. Moreover, the amount of installed capacitance in the second group is still exceedingly high, when the rated output frequency is relatively low.

A more recent proposal addressing this problem is the quasi-two-level PWM operation, first published in Ref. (11). This operation mode mimics the standard two-level voltage source inverter (VSI). In order to massively reduce the amount of installed capacitance in modules, the multilevel property of the MMC has to be sacrificed. Although this might seem as a large drawback at first sight, the inductance of a low-speed machine should be sufficient for the current filtering despite the quasi-two-level voltage shape. Moreover, as a trapezoidal (staircase) waveform is used instead of the rectangle form typical for a two-level VSI, the output voltage dv/dt is limited. This mitigates the critical problem of reflection due to long machine cables and thus significantly reduces the requirements on the machine isolation systems.

Therefore, the quasi-two-level PWM operation of an MMC is expected to be highly beneficial for cost-sensitive low-speed medium-voltage drives, as various nominal voltages are achievable using standardized low-cost modules with a very low amount of installed capacitance.

This paper investigates the application of the common-mode voltage (CMV) injection techniques, known from two-level VSIs, to quasi-two-level PWM-operated MMCs. First, the principle of the quasi-two-level PWM operation is explained in Section 2, and the trade-offs for maximum duty cycle, which have to be met during the design process, are derived in Section 3. The CMV injection techniques and their application to quasi-two-level PWM-operated MMCs are presented in Section 4. These are validated on a downscaled prototype (Section 5), and the simulations for different
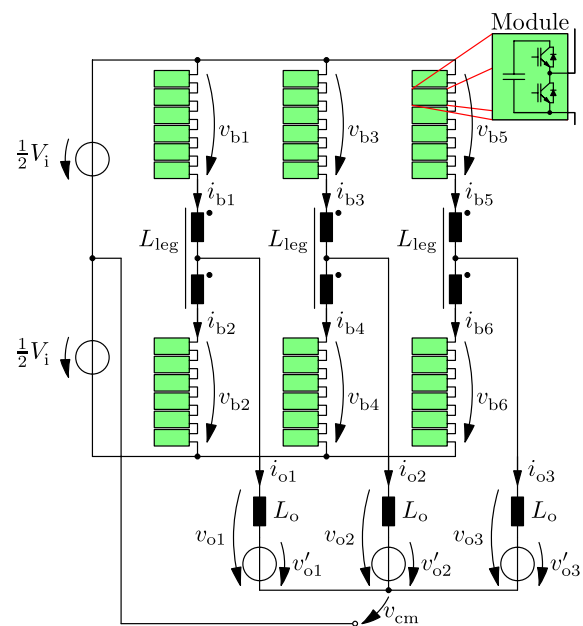
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Fig. 1.   Studied Modular Multilevel Converter

modulation indices and power factors are carried out. Finally, the results and their comparison are discussed in Section 6.

2. Quasi-Two-Level PWM Operation

The principle of the quasi-two-level PWM operation can be explained using Fig. 2. Because all three phase legs are identical and are controlled independently, it is sufficient to concentrate on the first phase leg consisting of branches 1 and 2, and (coupled) branch inductors.

As for two-level VSI, the output voltage is generated by a PWM, by comparing the carrier c_1 to the duty cycle δ_1 (as shown in the first graph of Fig. 2). When the duty cycle signal is higher than the carrier, the voltage of branch 2 v_{b2} approximates the input direct voltage V_i with high-frequency modulation (HF modulation), and all the modules of branch 1 are short-circuited ($v_{b1} = 0$). When the duty cycle signal is lower, branch 1 approximates the input voltage and branch 2 is short-circuited.

Between these two described states, transition states are applied, where either all modules of both branches are inserted or all modules of both branches are short-circuited. The purpose of the transition states is to change the leg current

$$i_{leg1} = \frac{1}{2} \cdot (i_{b1} + i_{b2}) \cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

as fast as possible.

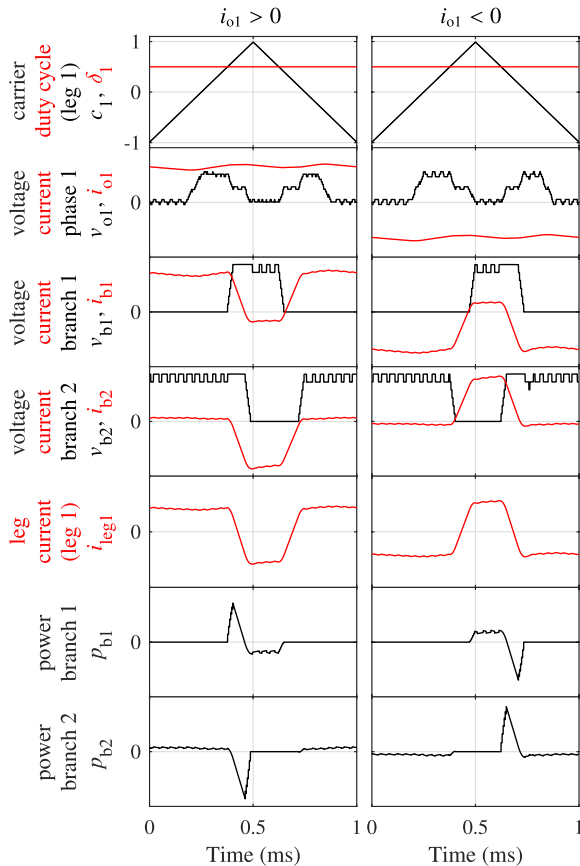In order to limit the dv/dt of the phase voltages and

Fig. 2. Quasi-two-level PWM operation example waveforms for positive and negative output current direction shown for one PWM period (1 ms)

common-mode voltage v_{cm}, a minimum delay is assigned between every two switching instants of the modules within one branch. This leads to a staircase shape of the branch voltages and the phase voltage v_{o1} in Fig. 2.

The branch voltages determine the waveform of the output (phase) voltage v_{o1}, which determines the output current i_{o1} (with the load inductance L_o and the load voltage v'_{o1}).

The main idea for reducing the energy variation in the modules' capacitors is to split the output current i_{o1} between the branches 1 and 2, so that the branch with currently short-circuited modules handles most of the current and the current of the branch generating a high voltage is very low. This current division is adjusted by the leg current (Fig. 2).

However, because of the staircase form of the branch voltages and the limited di/dt of the leg current, the branch powers (buffered in the module capacitors) cannot always be instantaneously zero. Consequently, power peaks appear in the branch powers (last two graphs of Fig. 2). These power peaks are then compensated by a small branch current in the opposite direction while the branch voltage is high. This current will be further referred to as "compensating current".

3. Design Trade-Offs for Maximum Duty Cycle

The closer the duty cycle is to 1 or −1, the shorter is the time period available for the power-peak compensation in one of the branches, leading to higher branch currents. This means that the maximum possible duty cycle is a design parameter influencing the leg inductance, the module capacitance, and the HF-modulation frequency. Below, the derivation of these relationships (and trade-offs) will be presented.

The energy disturbance Δe_b caused by the mentioned power peak can be calculated as a triangle area under the branch power waveform according to (2). The length of the triangle is the time period T_T needed for the transition state to finish. The height of the triangle is the branch-power peak value $\hat{p}_b$.

$$\Delta e_b = \frac{1}{2} \cdot \hat{p}_b \cdot T_T = \frac{V_b \cdot \hat{i}_b}{2} \cdot T_T \cdots\cdots\cdots\cdots (2)$$

The branch-power peak value can be calculated as a product of the peak branch current $\hat{i}_b$ and the maximum branch voltage V_b, when the staircase waveform of the branch voltage is simplified to a rectangle. The transition state duration

$$T_T = \frac{L_{leg} \cdot \hat{i}_b}{2 \cdot V_b - V_i} \cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

is dependent on the leg inductance of the coupled inductor L_{leg}, peak branch current $\hat{i}_b$, and the difference between the input voltage V_i and the sum of both branch voltages $2V_b$, Fig. 1.

As the maximum branch current, which can occur, is approximately the output current amplitude $\hat{i}_b \approx \hat{i}_o$ and the maximum branch voltage can be roughly approximated as input voltage $V_b \approx V_i$, a worst-case estimation of the maximum branch energy deviation

$$\Delta e_{b,max} \approx \frac{1}{2} \cdot L_{leg} \cdot \hat{i}_o^2 \cdots\cdots\cdots\cdots\cdots\cdots (4)$$

can be derived using (2) and (3).

Table 1. Converter Parameters

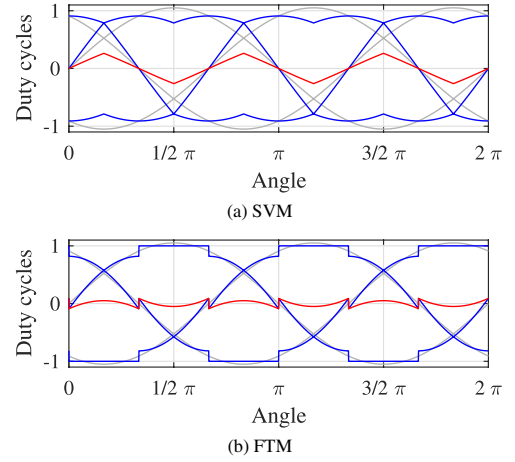| Parameter		Simulation	Prototype
Input voltage	V_i	4 kV	220 V
Output current amplitude	$\hat{i}_o$	400 A	22 A
Output power factor	$\cos\varphi_o$	1	0.996
Output frequency	f_o	5 Hz	5 Hz
PWM frequency	f_{PWM}	1 kHz	1 kHz
HF-modulation frequency	f_{HF}	25 kHz	25 kHz
Modules per branch	n_{mod}	6	6
Module capacitance	C_{mod}	0.2 mF	0.2 mF
Module setpoint voltage	V_C^*	720 V	40 V
Leg inductance (coupled)	L_{leg}	0.2 mH	0.2 mH
Load inductance	L_o	15 mH	15 mH
Energy storage constant	H	1.4 ms	1.4 ms

Fig. 3. Example duty-cycle waveforms, $M = 1.05$. Grey lines represent the setpoint sine duty cycles, red line the injected duty-cycle component, and the blue lines the resulting duty cycles used for the output PWM

This energy deviation has to be compensated with a compensating current, while the corresponding branch voltage is high. Its value is the highest ($\hat{i}_c$), when the time period for the compensation is the shortest ($T_{c,min}$):

$$\Delta e_{b,max} = V_i \cdot \hat{i}_c \cdot T_{c,min} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

The time available for the compensation

$$T_{c,min} = \frac{1 - \delta_{max}}{2} \cdot \frac{1}{f_{PWM}} \cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

is a function of the maximum duty cycle δ_{max} and the PWM frequency f_{PWM}, when the duration of the transition state is neglected.

Substituting (4) and (6) into (5), the maximum compensating current

$$\hat{i}_c = \frac{L_{leg} \cdot \hat{i}_o^2 \cdot f_{PWM}}{V_i} \cdot \frac{1}{1 - \delta_{max}} \cdots\cdots\cdots\cdots\cdots\cdots (7)$$

can be expressed as a function of the leg inductance and the maximum duty cycle. This equation shows that for a given input voltage V_i, PWM frequency f_{PWM}, and output current amplitude $\hat{i}_o$, the higher the maximum duty cycle δ_{max} is required, the higher the maximum compensating current $\hat{i}_c$ or the lower the inductance of the leg inductor L_{leg} has to be. However, both scenarios are undesired, as a higher compensating current leads to higher semiconductor losses and a lower inductance requires a higher HF modulation frequency in order to keep the leg-current ripple limited. Moreover, when the maximum duty cycle approaches one, the HF modulation frequency or the compensating current would approach infinity. Therefore, the duty cycle must necessarily be limited to a value below one.

Note that the duty cycles being exactly 1 or −1 are also achievable, as these do not cause any power peaks, and therefore, no compensation is necessary.

Equation (7) also implies that it is allowed for the duty cycle to exceed its designed maximum value, if the output current is reduced at these operating points accordingly. This option is not further studied in this paper.

Considering the derived trade-offs, the converter presented in this paper has been designed for a maximum duty-cycle value limited to 0.9. This limits the maximum compensating current to 20% of the nominal output-current amplitude, regarding the parameters in Table 1.

4. CMV Injection Techniques

The basis for the injection techniques is to modify the setpoint duty-cycle vector $\boldsymbol{\delta'} = [\delta'_1, \delta'_2, \delta'_3]$, in order to improve some properties of the converter [12]. The resulting duty-cycle vector $\boldsymbol{\delta}$ used for the PWM is obtained by adding the common-mode component δ_{cm} to the setpoint duty-cycle values for each phase δ'_1, δ'_2 and δ'_3:

$$\boldsymbol{\delta} = [\delta_1, \delta_2, \delta_3] = [\delta'_1 + \delta_{cm}, \delta'_2 + \delta_{cm}, \delta'_3 + \delta_{cm}] \quad \cdots\cdots (8)$$

One obvious option is not to inject any common-mode component:

$$\delta_{cm}^{SM} = 0 \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (9)$$

This technique is also referred to as "Sine Modulation" (SM).

The second option is to apply the "Carrier-Based Space-Vector Modulation" (SVM) with

$$\delta_{cm}^{SVM} = -\frac{\max(\boldsymbol{\delta'}) + \min(\boldsymbol{\delta'})}{2} , \cdots\cdots\cdots\cdots\cdots (10)$$

extending the maximum modulation index M without overmodulation. This technique is similar to the "Third-Harmonic Injection". However, it has a significant advantage, as the output angle does not have to be known to calculate the injected component. Therefore only SVM is investigated. Waveforms demonstrating the technique are plotted in Fig. 3(a).

The third investigated technique is the "Flat-Top Modulation" (FTM), also called "Discontinuous Modulation", shown in Fig. 3(b). This technique does not only extend the maximum modulation index, but it also reduces the switching losses, as the converter's phase leg does not have to switch when the duty cycle is 1 or −1. The injected common-mode component can be calculated as:

$$\delta_{cm}^{FTM} = \text{sign}\left(\max(\boldsymbol{\delta'}) + \min(\boldsymbol{\delta'})\right)$$
$$\cdot \left(1 - \max(\text{abs}(\boldsymbol{\delta'}))\right) \cdots\cdots\cdots\cdots\cdots (11)$$

In literature, modified variants of this technique can be found [13], which shift the position of the "flat top" according to the output current to further reduce the switching losses, when the output current is not aligned with the output voltage. However, the optimum shift has to be searched for each

modulation index and power factor and its value changes in dependency on the maximum duty cycle achievable with the converter. Thus, only the described (simple) method will be further investigated in this paper.

As explained in Section 3, the maximum duty cycle of the quasi-two-level PWM-operated converter is limited (e.g. to 0.9 with presented converter) except for the duty cycle being exactly 1 or −1. In Fig. 4, the maximum required duty cycle (excluding 1) is plotted in dependence on the modulation index. Using this figure and assuming a maximum duty cycle of 0.9, we can state that the maximum achievable modulation index with SM of 0.9 can be extended to ≈ 1.05 with SVM and even to ≈ 1.1 with FTM.

To improve the properties of the FTM with a quasi-two-level PWM-operated MMC, it is recommended to inverse the carrier function for a particular converter phase x, if its required duty cycle δ_x is lower than zero.

This can be explained using Fig. 2. Observing branch voltage 1, it can be recognized that its values change from zero to high voltage and then back to zero during each PWM period. In contrary, the branch voltage 2 is firstly high, then zero, and afterwards high again. If the next required duty cycle is 1, the branch voltage 1 remains zero and the branch
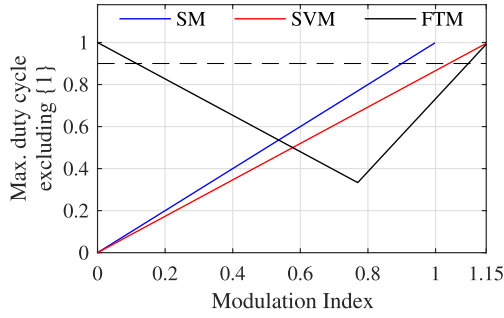
voltage 2 remains high, leading to a fluent transition without any additional switching. However, if the next required duty-cycle value is −1, both branch voltages must be changed. It leads to additional switching and significant branch energy disturbances, since additional branch power peak occurs, as demonstrated in Fig. 5(a). This can be prohibited simply, when the described PWM pattern is inverted for negative duty cycles, leading to a fluent transition to and from the state of duty cycle being −1. The simplest way to do so is by inverting the corresponding carrier, as shown in Fig. 5(b).

5. Simulation Model and Its Experimental Validation

The simulation model used for the investigations was implemented in Matlab/Simulink, using Plecs toolbox for the electrical part of the model. The converter input source was

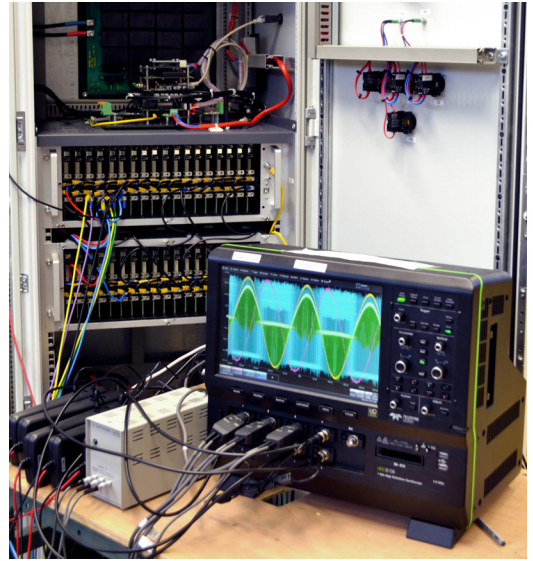Fig. 4. Analytical comparison of the considered injection techniques

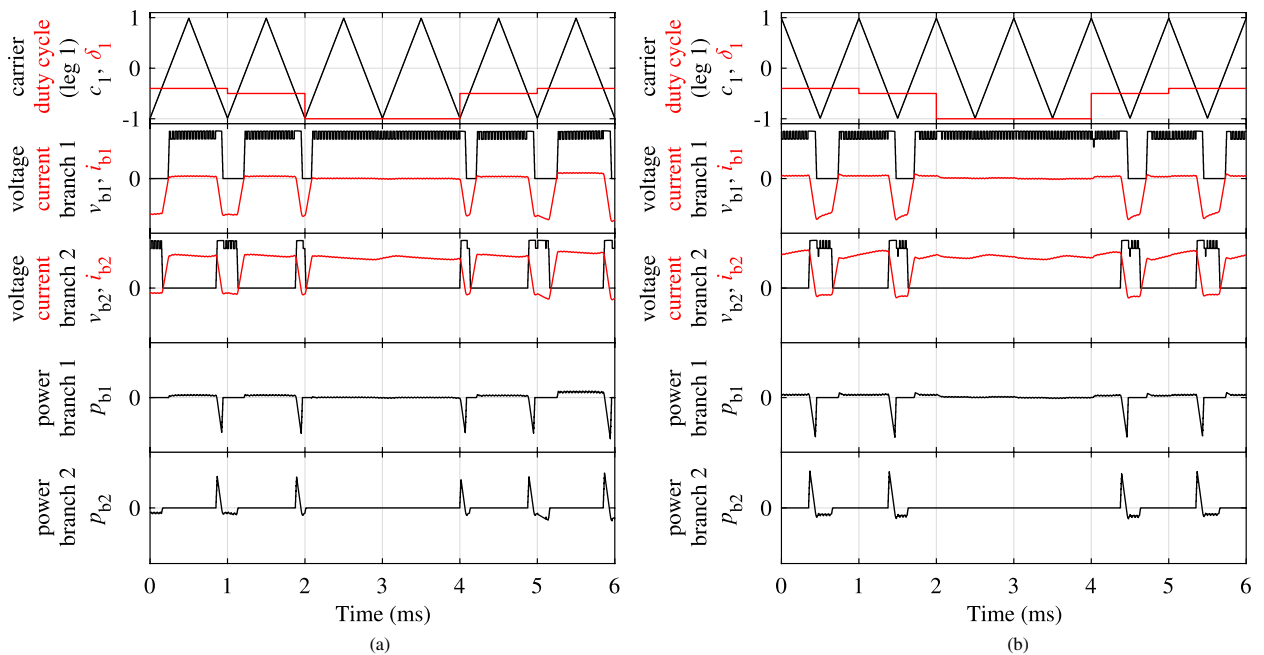Fig. 6. Photo of the downscaled converter prototype

Fig. 5. Demonstration of the FTM for negative duty cycles with (a) non-inverted carrier (b) inverted carrier
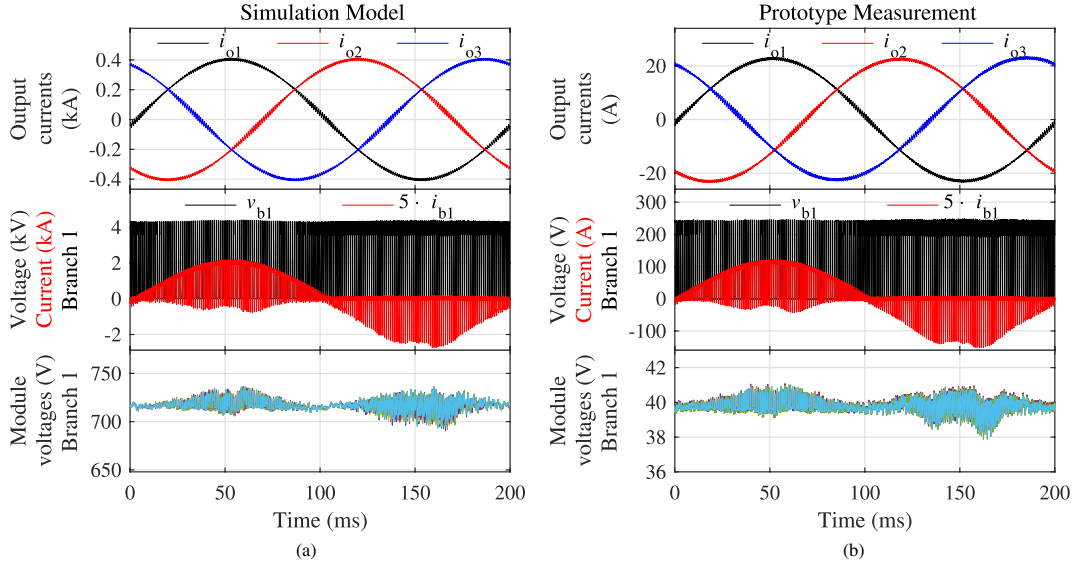
Fig. 7. Experimental validation of the quasi-two-level PWM-operated modular multilevel converter with SVM, $M = 1.05$: (a) simulated waveforms (b) measured waveforms on downscaled prototype
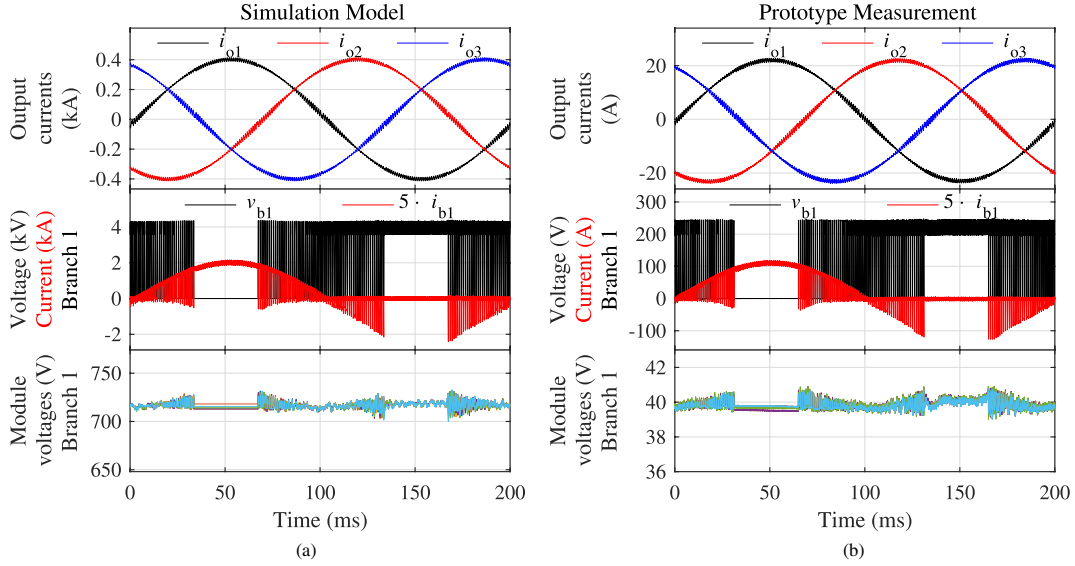

Fig. 8. Experimental validation of the quasi-two-level PWM-operated modular multilevel converter with FTM, $M = 1.1$: (a) simulated waveforms (b) measured waveforms on downscaled prototype

assumed to be a direct-voltage source. The converter output was connected to an alternating-voltage source, controlling the fundamental harmonic of the output current with a very slow proportional-resonant controller. The voltage THD of this voltage source was under 0.5% in all operating points and therefore, the higher output current harmonics were influenced almost exclusively by the converter itself. The simulation parameters are summarized in Table 1. The converter's energy storage time constant H (the total energy stored in the modules' capacitors divided by the maximum converter power) was calculated, assuming the maximum modulation index is 1.1. The loss calculation is based on the IGBT/Diode module `Infineon FZ400R12KE4` [14].

In order to validate the simulation model, a downscaled experimental prototype was developed, Fig. 6. In reference to the simulation model, the prototype is scaled down by a factor of 18 for currents and voltages, Table 1. In Fig. 7, the simulation results and prototype measurements are plotted,
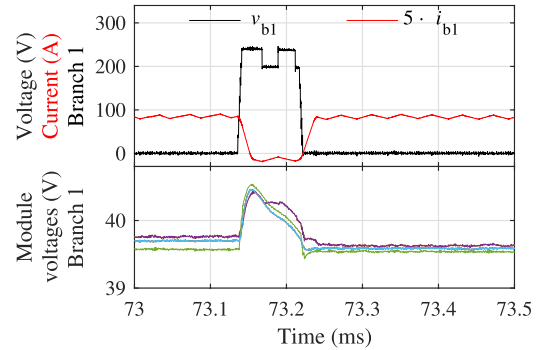

Fig. 9. Measured detail of the quasi-two-level PWM operation (Fig. 8(b) zoomed in; the branch current and the branch voltage are not filtered)

showing the operation with SVM. In Fig. 8, the operation with FTM is shown. The measured waveforms are zoomed in in Fig. 9. For a better correspondence, both the simulation
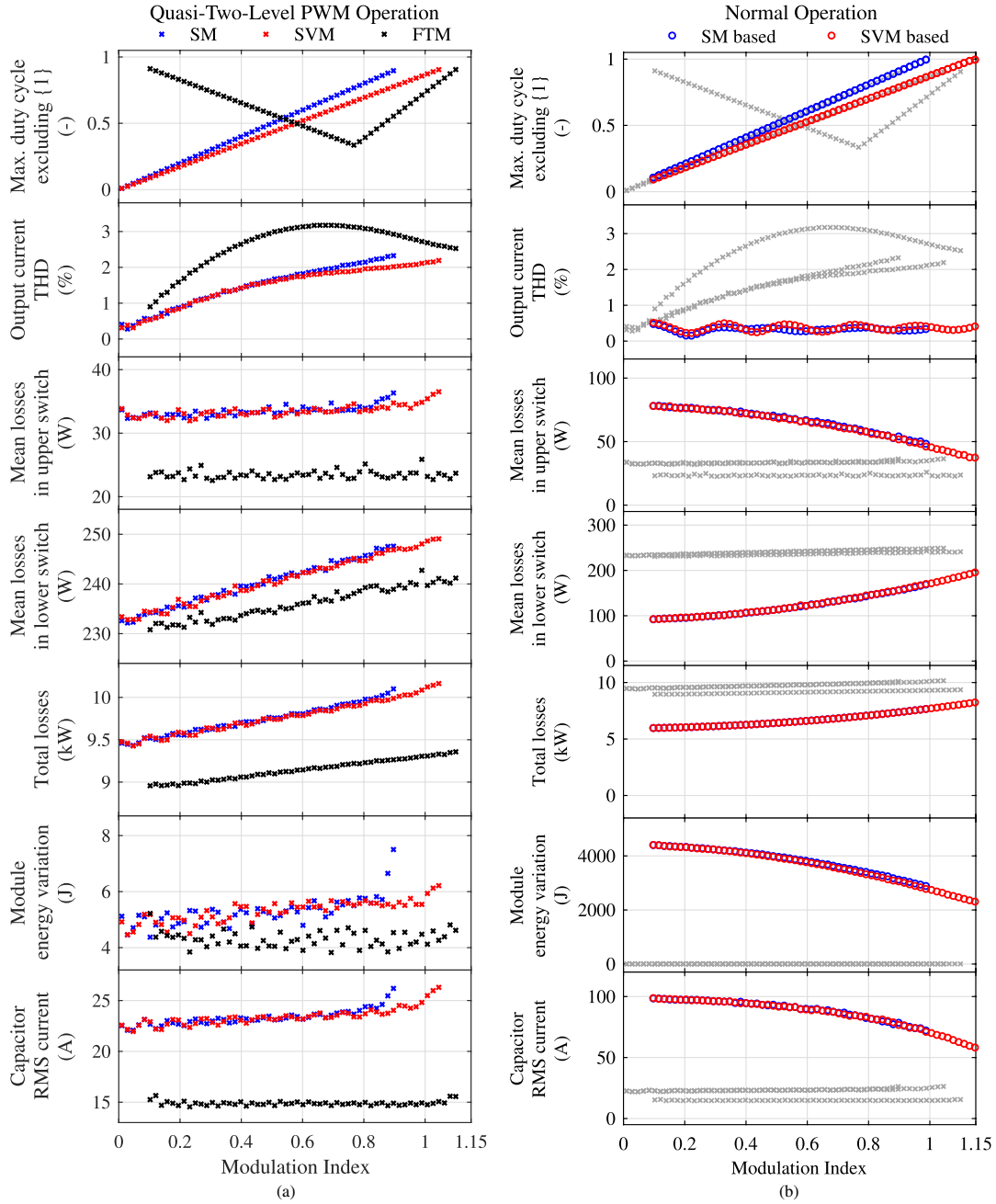
Fig. 10. Comparison of the injection techniques in dependence on modulation index with a constant output current and unity power factor: (a) quasi-two-level PWM operation, (b) normal operation mode – the grey "x" markers represent the quasi-two-level PWM operation data (for a better correspondence). The values of the mean losses, the energy variation and the capacitor current are given for the worst-case module during one simulated period (200 ms)

and the measurements employ a resistor instead of the voltage source as a load. With downscaled prototype, only three module capacitor voltages (out of six) were measured. To reduce the signal noise in measurements due to EMI, the measured waveforms are filtered with an 1 MHz low-pass filter. In general, a very good correspondence between the waveforms can be stated and thus the simulation models are valid.

6. Comparison of Results

In Fig. 10(a), the steady-state simulation results are plotted as a function of the modulation index for different injection techniques. The output current amplitude is kept constant at 400 A (see Table 1) with unity power factor. In the first graph,

the maximum duty cycles are plotted, confirming the findings from Fig. 4. It can also be seen that the maximum duty cycle was limited to 0.9. While the properties of the SVM and SM are almost identical (except for the extended modulation index with SVM), the FTM has a significant influence on all parameters. The first visible change is the significantly higher THD representing the output current ripple. Secondly, the semiconductor losses are lower, since less switching instants are necessary. Thirdly, the energy variation in the module capacitors and (consequently) the RMS value of module capacitor currents are lower.

However, the unity power factor, selected for the investigations in Fig. 10(a), is the best case for the FTM. In Fig. 11(a),
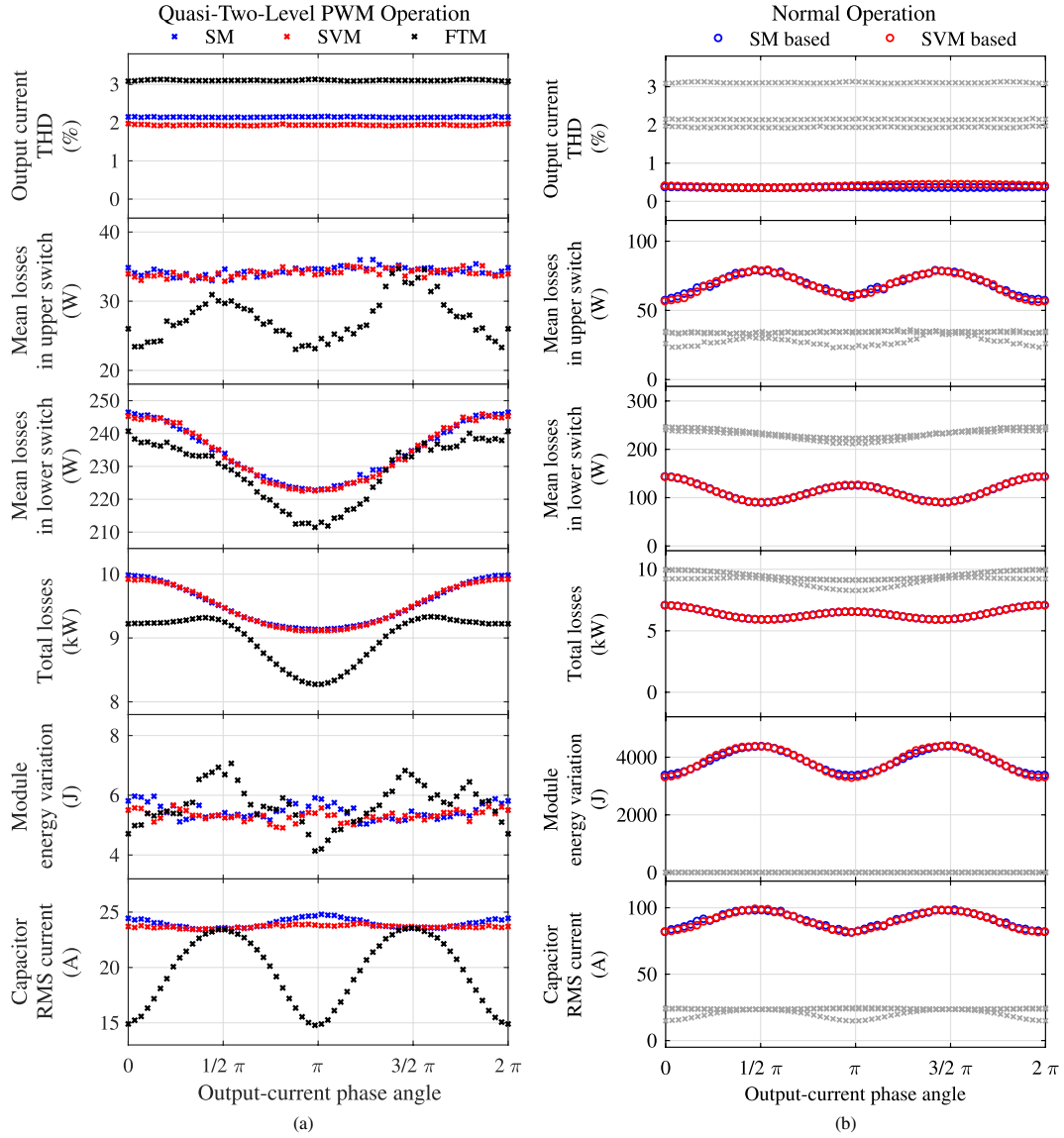
Fig. 11. Comparison of the injection techniques in dependence on the output-current phase angle φ_o with a constant output-current amplitude and modulation index $M = 0.8$: (a) quasi-two-level PWM operation, (b) normal operation mode – the grey "x" markers represent the quasi-two-level PWM operation data (for a better correspondence). The values of the mean losses, the energy variation and the capacitor current are given for the worst-case module during one simulated period (200 ms)

the dependencies on the output-current phase angle φ_o for a constant modulation index $M = 0.8$ are plotted. As can be observed, the converter losses and the capacitor RMS currents are close to those of SM or SVM modulated converter, when reactive power is required at the converter output. Moreover, when only reactive power is required (φ_o is $\frac{1}{2}\pi$ or $\frac{3}{2}\pi$), the module energy variation with FTM becomes worse than the one of SM or SVM. This is caused by carrier signals being inverted while the branch current is the highest.

Furthermore, Fig. 11(a) shows that the quasi-two-level PWM operation leads to lower losses in the module's lower IGBT/diode switch, when the active power is transmitted from the load. The cause is the shorter time in which the IG-BTs conduct the branch current and the longer time in which the diodes conduct it.

In general, considering both Fig. 10(a) and Fig. 11(a), it can be stated that the upper IGBT/diode switch in the module has significantly lower losses than the lower switch and

therefore could be designed smaller, thus reducing the semiconductor costs and switching losses.

The investigations from Fig. 10(a) and Fig. 11(a) have also been accomplished in normal converter operation mode. The results are shown in Fig. 10(b) and Fig. 11(b), respectively. For a better correspondence to quasi-two-level PWM operation, the data from Fig. 10(a) and Fig. 11(a) are plotted as grey "x" markers. As significantly higher energy variation per module occurs in the normal operation mode, the module capacitance was increased to 200 mF (the energy storage constant was increased to 1.35 s, assuming the maximum modulation index is 1.15). The modulation (and control) frequency was chosen at 1 kHz, being identical with the PWM frequency of the quasi-two-level PWM-operated MMC. The leg inductance was increased to 12 mH, accordingly.

While slightly higher modulation indices are reachable in normal operation mode, and the current distortion is significantly lower (as expected), the total energy variation,

representing the amount of installed capacitance in the modules, is up to 850 times higher. Additionally, the module capacitors are loaded with significantly higher RMS currents. The converter losses are generally lower in normal operation mode, as this leads to a lower number of switching instants, since the number of levels switched each modulation period is lower. Nevertheless, the difference is relatively small despite the relatively low modulation frequency (1 kHz), chosen for the normal operation mode. This is also partly caused by the fact that the HF-modulation does not contribute to the switching losses significantly, since it is only applied, when the according branch current is low. Moreover, the advantageous efficiency of the normal operation mode is expected to be diminished in drive applications during operation at machine speeds below nominal, when high-frequency CMV injection and additional circulating currents have to be applied.

7. Conclusions

In this paper, three different injection techniques applied to the quasi-two-level PWM-operated MMC were studied and compared. It can be concluded that all three techniques are feasible, which has also been validated on an experimental converter prototype.

As could be derived in this paper, the achievable modulation indices with the quasi-two-level PWM operation are limited to some value below one, if no CMV injection is applied (the case of SM). The SVM technique extends the maximum achievable modulation index by a factor of ≈ 1.15 in comparison to SM, while the other important properties remain unchanged. The FTM technique can further extend the modulation index and additionally reduce the converter losses; however, it leads to higher output-current distortion. Therefore, it is recommended to use the SVM technique by default. The FTM technique can be optionally used for higher modulation indices, if the additional current distortion is acceptable.

The comparison to the normal operation of MMC confirmed the expected advantages of the quasi-two-level PWM operation (i.e. significantly lower module capacitance requirements) and its disadvantages (i.e. higher current distortion and losses).

Additionally, the paper has shown that the upper IGBT/diode switch in modules has significantly lower losses than the lower switch, when the quasi-two-level PWM operation is applied. In future work, the option to decrease the size of this switch will be investigated. Furthermore, the control implementation used for the converter prototype will be presented and the application of quasi-two-level PWM-operated MMC to medium-voltage low-speed drives will be studied more extensively, drawing a comparison to other converter topologies and operation modes.

Acknowledgment

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