IEEJ Journal of Industry Applications
Vol.8 No.2 pp.379–385 DOI: 10.1541/ieejjia.8.379
Translated from IEEJ Transactions on Industry Applications, Vol.138 No.8 pp.669–675

Paper
(Translation of IEEJ Trans. IA)

A Completely Capacitor-less, LED-switching Offline Lighting System

Kenji Yamamoto[*a)] Member, Richard Lum[**] Non-member
Hisashi Takahashi[*] Senior Member

Recently LED lighting apparatus are becoming more popular and well received by users. An offline LED apparatus needs to have electrolytic capacitors inside to supply LEDs with a regulated DC voltage. Although LEDs are characterized by longevity, the shorter lifetime of the constituent electrolytic capacitors limit the lifetime of the LED lighting apparatus. That means that actual LED lifetime is being wasted, consequently wasting the manufacturing cost. This paper proposes a new LED drive circuit topology, which does not need any electrolytic capacitors and shows the simulation results of the circuit. Also described are simulation results of its efficiency, the power factor, and EMC characteristics without any reactance at the line interface. From the simulation results, it is shown that the circuit topology has the potential for practical use.

Keywords: light emitting diode, LED, LED lighting, offline LED driver, LED switching, electrolytic capacitor-less

1. Introduction

Lighting apparatus that use light emitting diodes (LEDs) have spread rapidly since the 2010s and have now become a popular choice among lighting fixtures in recent years [(1)].

Because LEDs are constant-voltage elements, a direct electric current is necessary which then calls for a rectifier and a smoothing circuit. The life-span of the electrolytic capacitors used in smoothing circuits less than that of LEDs, thus the life-span of the LED light fixture is governed by the electrolytic capacitor. To resolve the issue of electrolytic capacitors limiting device life-spans, an offline LED power source with PFC circuit action has been proposed; however, the complexity of the circuit format and the **subsequently** increased loss of the switching elements and the reactor's internal resistance are problematic [(2)].

Several methods involve omitting electrolytic capacitor and changing the number of series connections in response to changes in the power source's voltage, as LEDs are constant voltage elements [(3)–(8)]. These methods show relatively favorable values for power factor and efficiency. However, complete omission of an electrolytic capacitor was not possible because the methods use an enhancement-mode FET to control the transistor which controls the LED current. This necessitates a gate-drive power source which needs an electrolytic capacitor [(9)(10)]. This proposal simplified the circuit by using a depletion-mode FET and employing a low-power comparator IC to remove gate-drive power source and control power source. The proposed circuit's operation was confirmed via simulation in which it demonstrated satisfactory efficiency. Compliance to an harmonic and electromagnetic interference standard was demonstrated by adding a current limit circuit and modulating the voltage reference circuit which determines the activation timing for the dual LED string configuration. This was confirmed via simulation in which it fulfilled conducted emission requirements.

a) Correspondence to: Kenji Yamamoto. E-mail: yamamoto.kenji@sist.ac.jp
* Graduate School, Shizuoka Institute of Science and Technology 2200-2, Toyosawa, Fukuroi, Shizuoka 437-8555, Japan
** Jalan Korban, Singapore

2. Proposed Circuit Concept

2.1 Basic Structure of the Conceptual Circuit

Figure 1 shows the basis structure for the conceptual circuit. The bridge rectifier conducts full wave rectification of the commercial power source voltage v_{line} and receives the full-wave rectifier voltage v_{rect} and supplies this to the LED

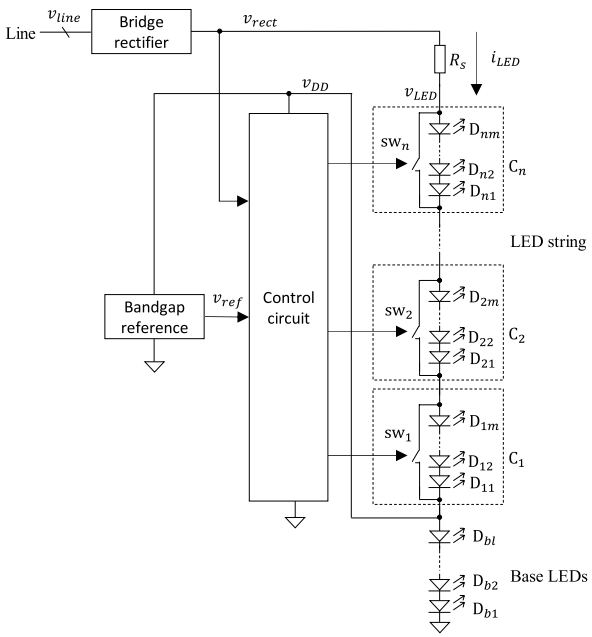


Fig. 1. Conceptual circuit diagram of the proposed LED switching lighting system

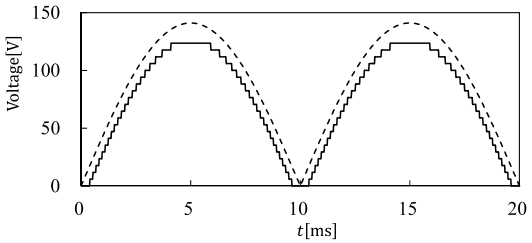
string and the control circuit. Rs is the current-limiting resistor which restricts the current influx to the LED string.

The LEDs m inside of the series circuit and the set of switches connected to both of their ends sw_k ($k = 1 \sim n$) are referred here as cells. N is the number of cells. LEDs l (D_{bk}, $k = 1 \sim l$) are connected in the lower portion of the LED string. These LEDs are called the base LEDs.

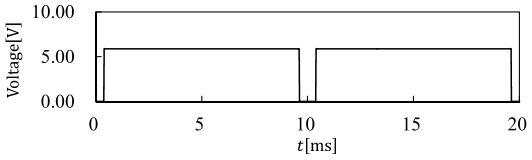
The control circuit constitutes a series LED circuit that enables an appropriate LED current (I_{LED}) to be received in response to the instantaneous value of v_{rect}. The control circuit does this by handling the switches, comparing the reference voltage v_{ref}, which is produced by the bandgap reference and the full-wave rectifier voltage v_{rect}, and short circuits the appropriate number of LEDs from the LED string.

The voltage produced in any of the anode terminals of D_{bk} is used as the control circuit and bandgap reference power source v_{DD}.

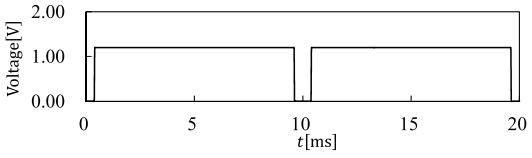
Figure 2 shows the ideal operation wave for each part of Fig. 1. The conditions in this case are shown Table 1. The supply voltage v_{DD} is received from anode terminals D_{b2}. Figures (a)–(d) show a 20 ms interval with a line frequency of 50 Hz, the horizontal axis representing time. Figure (a) shows the full-wave rectifier voltage v_{rect} and the voltage drop of the LED v_{LED} string. These differences in potential difference results in a voltage drop at the current-limiting resistor R_s.



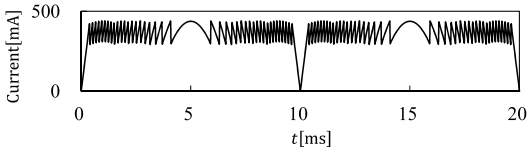
(a) Rectified voltage v_{rect} (dotted line) and LED string voltage v_{LED} (solid line)



(b) Power supply voltage v_{dd}



(c) Reference voltage v_{ref}



(d) LED current i_{LED}

Fig. 2. Ideal waveforms of the conceptual circuit diagram

Table 1. Parameter values for conceptual model of Fig. 1 and Fig. 2

Parameter	Description	Value
l	N of base LEDs	2
m	N of LEDs in a Cell	2
n	N of Cells	23
V_F	Forward voltage drop of an LED	2.94[V]

Figures (b) and (c) are graphs of the power source v_{DD} and the reference voltage v_{ref}, respectively. These voltages are not generated in the vicinities of t = 0, 10, 20 [ms], which are sections where v_{rect} is lower than the voltage drop than the series connection of D_{b1}-D_{bl}. Thus, supply voltage is not supplied to the bandgap reference and control circuit. In this case, all switches are designed to close.

The mechanism for judging the addition of open switches according to the full-wave rectifier is governed by the formula below:

$$v_{rect} > m(c+1)V_F + lV_F$$

Here, c is the number of opened cells and V_F is the LED voltage drop. The first item near the right is the voltage drop of all cells when a new switch is opened. The second item is the voltage drop of the base LEDs.

Figure (d) is the current flowing to the LED string i_{LED}. The control-limiting resistor R_s and the operation of the switch groups by the control circuit controlled by i_{LED} = 300 mA–450 mA.

2.2 Practical Example of Circuit The circuit used in the simulation is shown in Fig. 3. This circuit short circuits the appropriate number of cells by the FETs (referred to as shunt FETs in this essay) connected in parallel to the cells by comparing the voltage of the full-wave-rectified commercial power supply (Line) at the diode bridge v_{rect} to the reference voltage v_{ref}. There are two LEDs within the cell.

The shunt FET, the shunt FET drive circuit, the circuit with the comparator C1-C_n are referred to as cells in this example. The number of cells in this manuscript's simulation is n = 23. There are 2 base LEDs. Resistive divider 1 divides the voltage of v_{rect} into an easily comparable voltage using the cell circuit. Resistive divider 2 divides the voltage of v_{ref} into an appropriate voltage. When compared to resistive divider 2, it provides an appropriate voltage to each cell comparator to open each cell's shunt FET. The current limiting resistor R_s

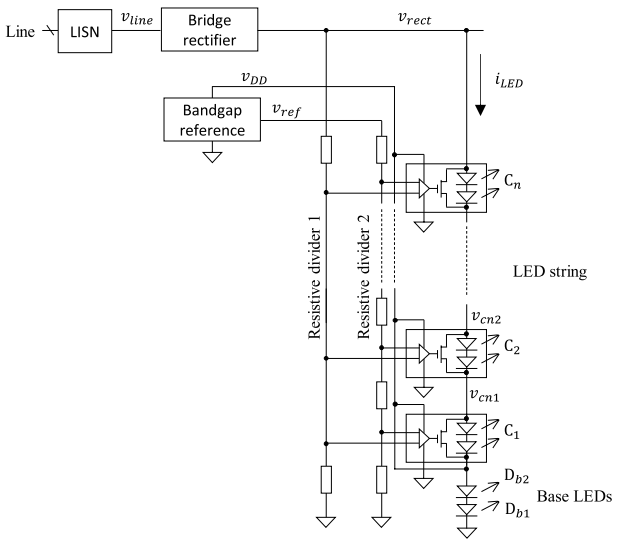


Fig. 3. Simulated circuit of the proposed conceptual model

is omitted in this example, because when every shunt FET is conducted, the drain-source resistance remains.

The power sources for the bandgap reference circuit and the comparator for every cell is the voltage drop v_{DD} of the final (2) base LEDs connected to the grounded side of the cell, as explained before. Power is not supplied when v_{rect} is lower than the voltage drop of these LEDs because this voltage is not smoothed. The FETs that short circuit the LEDs use a n-type depletion FET; when power is not supplied, the LED strings in all cells are shorted. The output of the bandgap reference v_{ref} needs to be established before the full-wave rectifier voltage v_{rect} first reaches the voltage where it should open the shunt FETS after establishment of the power source voltage v_{DD}. This is identical to the operation establishment period of the control circuit.

The line impedance stabilization network (LISN) connected between the commercial power supply (Line) and the bridge rectifier was inserted for an impedance model for a commercial power supply circuit network.

2.3 Cell Circuits The cell schematic is shown in Fig. 4. D1 and D2 are LEDs. M1 is the enhancement-mode FET and M2 is the depletion-mode FET. Reference voltage v_{ref} used a voltage from a reference voltage source of about 1.2 V built into the comparator ICs (U1). In each of the comparator ICs (as many as there are cells) there is a bandgap reference circuit built-in. This was used to share the bandgap reference voltage v_{ref} of one cell comparator's IC.

When the comparator IC detects an appropriate voltage to light the cell LEDs, M2 is cutoff and current flows to D1 and D2 and illuminates them.

2.4 Simulation Results

(1) The circuit configuration shown in Figs. 3 and 4 were used in a simulation. The component model used in the simulation is shown in Table 2. Linear Technology's LTspice XVII(x64) [14] was used for the simulation. Figure 5 shows the waveform of the simulation results. Figure (a) shows the line voltage wave form after the rectifier $v_{rec}t$ which is in Fig. 5 and the anode potentials of the anode potentials of the LEDs in cells C6 and C17 (vcn6 and vcn17, not displayed in Fig. 3) as an example of the internal voltages of the LED string. Figure (b) shows the waveform of the LED string's current i_{LED}. The spike waveform produced in v_{rect} is the voltage waveform produced by the LISN circuit reactor and the voltage fluctuation caused when the LED current switches. The asymmetry seen in the LED string waveform, when the rectified line voltage rises and drops, is due to the asymmetry of the shunt FETs action speed due to a Miller effect.

Figure 6 shows the simulation results of v_{rect}, v_{DD}, and v_{ref}. It is evident that v_{ref} is established before the voltage of v_{DD} is established.

(2) The apparent power, power factor, efficiency and total power consumption from the simulation in Fig. 3 are shown in Table 3. Efficiency was obtained by P_{LED}/P_t; a ratio of the power consumption of all LEDs P_{LED} to the power consumption of all circuits P_t.

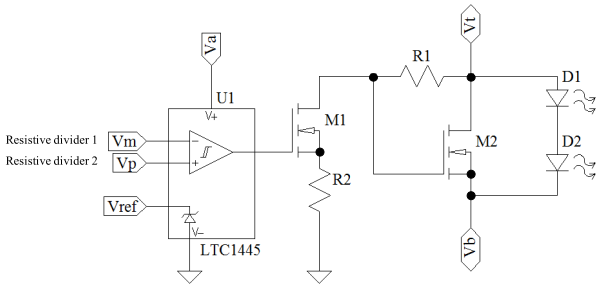
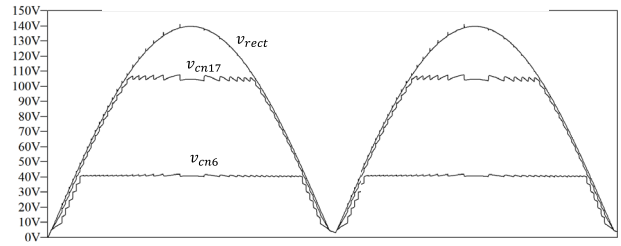


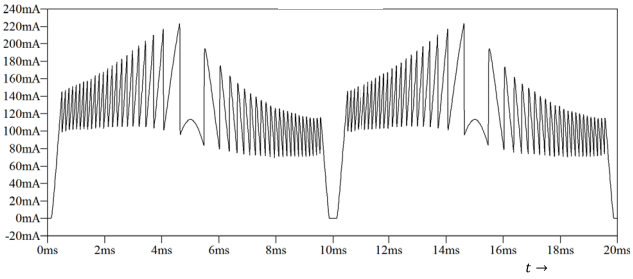
Fig. 4. Schematics of an LED drive cell

Table 2. Component models used in simulations

Designator	Manufactorer's part number	Description
M1	ZVNL120A	N channel MOS FET, enhancement
M2	BSP149	N channel MOS FET, depletion
D1, D2	W5AP-LZMZ-5K8L	Light emitting diode, white
U1, Bandgap reference	LTC1445	Four comparators with a reference voltage source

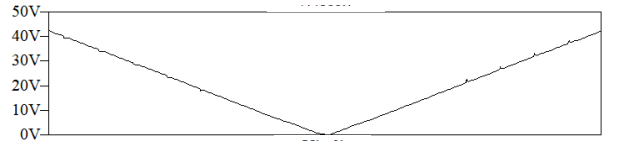


(a) Rectified voltage v_{rect} and LED string voltage v_{cn6} and v_{cn17}

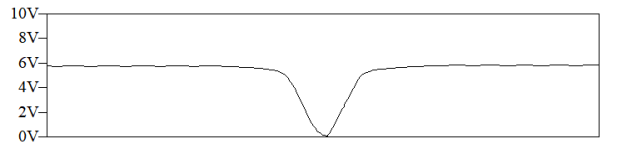


(b) LED string current i_{LED}

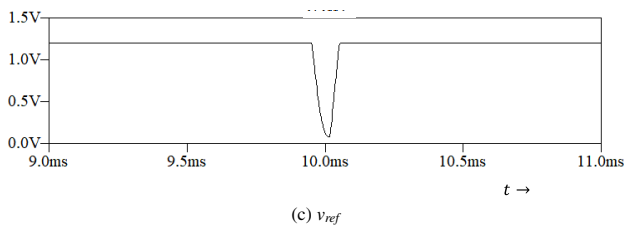
Fig. 5. Simulation results of Fig. 3, LED string voltages and current



(a) v_{rect}



(b) v_{DD}



(c) v_{ref}

Fig. 6. Simulation results of Fig. 3, $v_{rect} \sim 0$

Table 3. Simulation results of Fig. 3

	Simulation result	Unit
Total power consumption, P_t	11.6	W
Apparent power consumption	12.5	W
Power consumption in LEDs, P_{LED}	10.8	W
Power factor	0.929	
Efficiency	93.3	%

3. EMC Compliance

3.1 EMC Regulations EMC Regulation The EMC regulations applied to LED lighting apparatus are shown in Table 4 [11][12].

Harmonic current regulations (JIS C 6100- 3-2) stipulate the strength of harmonic currents for power frequency components. Radio interference regulations (CISPR15) are regulations on the superimposed voltage strength on power lines from radio frequencies. An emissions simulation was conducted from these regulatory values.

An LISN [13], shown in Fig. 7, is inserted in the circuit that provides electric power to the conceptual circuit. While EMCCOM is a joining terminal for common potential, the common mode impedance value depends on the packaging design. As such, it was assumed open in the simulation configuration. Common mode noise was not included in the simulation for this reason. For the two resistors (designators R1 and R2), one of the two was made into the input resistor for the voltmeter and the other acted as a dummy resistor that maintained the balance of the measurement system. The utility frequency was set to 50 Hz.

3.2 EMC Simulation Results of the Conceptual Circuit Table 5 shows the regulation values along with the simulation results for the conceptual circuit's (Fig. 3) EMC regulation values. There is little allowance for the third harmonic when trying to comply with harmonic current regulations. Also, while the regulatory values for fifth, ninth, and the eleventh harmonics onwards are not met, it demonstrated satisfactory results in accordance with radio interference regulations.

3.3 Circuit Configuration for EMC Compliance To address the criteria not met in the simulation results,

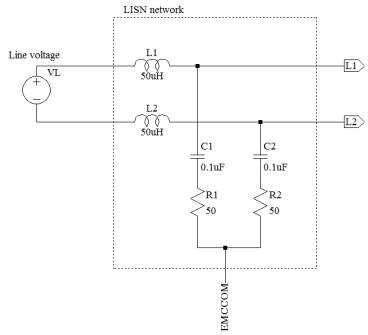


Fig. 7. Schematics of LISN

Table 4. Japanese EMC regulations applicable to lighting apparatus

Regulation Category	Regulation	Description	Concerned measure	Simulated in the paper
Harmonic current emission	JIS C 6100-3-2	Electromagnetic compatibility (EMC) -- Part 3-2: Limits -- Limits for harmonic current emissions (equipment input current <=20 A per phase)	Conducted harmonic current emissions	Yes
Emission of radiofrequency	CISPR15	Limits and methods of measurement of radio disturbance characteristics of electrical lighting and similar equipment	Conducted noise voltage	Yes
			Radiated magnetic field	
			Radiated electric field	

Table 5. Simulation results for Fig. 3 and regulatory limits

Regulation Category	Regulation	Frequency range	Limit	Simulation result	Margin
Harmonic current emission	JIS C 6100-3-2	2nd harmonic	-34dBc	-40dBc	6dB
		3rd harmonic	-(10.5dBc+20log$_{10}\lambda$)[(a)]	-12dBc	0.6dB
		5th harmonic	-20dBc	-18dBc	-2dB
		7th harmonic	-23dBc	-30dBc	7dB
		9th harmonic	-26dBc	-23dBc	-3dB
		11th to 39th harmonic	-30dBc	-25dBc	-5dB
Emission of radiofrequency	CISPR15	9kHz～50kHz	110dBμV	76dBμV	34dB
		50kHz～150kHz	90~80dBμV[(b)]	74dBμV	6dB
		150kHz～500kHz	66~56dBμV[(b)]	64dBμV	3dB
		500kHz～5MHz	56dBμV	36dBμV	20dB
		5MHz～30MHz	60dBμV	-6dBμV	66dB

dBc: Ratio of the noise voltage to the line frequency component, (a)λ is the power factor, assumed to be 0.9, (b)The limit decreases linearly as the logarithmic value of frequency increases.

which were mentioned in the previous paragraph, the following 3 changes were made to the conceptual circuit.

（1） Parallelization of the LED String The cause of the narrow margin of allowance for the third harmonic current regulation value is possibly because the current becomes 0 in the section where the voltage after bridge rectification is lower than the voltage drop of the two. To reduce the third harmonic, the current change on both sides of this section was smoothed by adding a parallel LED string which acts as a continually cut off shunt FETs at cells C1-C5 to the conceptual circuit as shown in Fig. 8.

（2） Peak Current Limiter To reduce the harmonic current at relatively high frequencies and radio interference, a current limiting circuit (Fig. 8; M13, R11, M23, R21) is installed in each LED string to suppress the transitional peak current.

（3） Addition of Noise to the Comparison Voltage An attempt was made to dissipate the harmonic's peak voltage into sideband waves by adding a noise voltage v_n to the reference voltage to the comparator (Fig. 8). The noise voltage simulation model is shown in Fig. 9(a). Figure (b) shows the noise voltage waveform. Noise voltage was further configured so that the peak voltage would be equal to the appropriate voltage needed to light one cell LED.

3.4 EMC Simulation Results of the EMC Compliant Circuit Table 6 shows the results of the simulation in which the EMC measures mentioned in the previous paragraph were performed. The numbers (1), (2), and

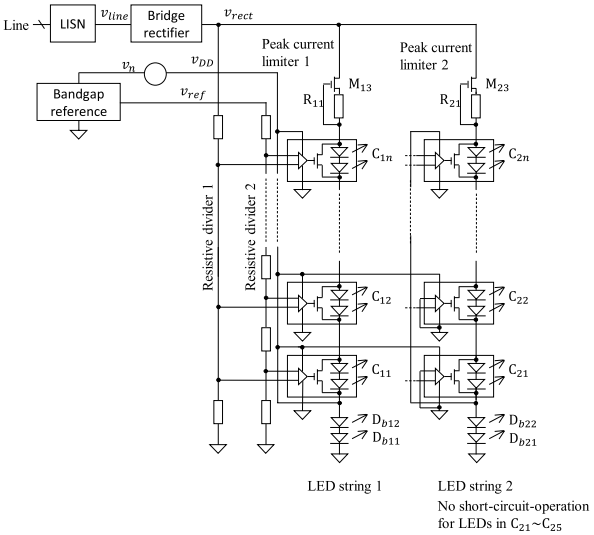


Fig. 8. EMC measures: 2nd LED strip, noise voltage v_n, and peak current limiters

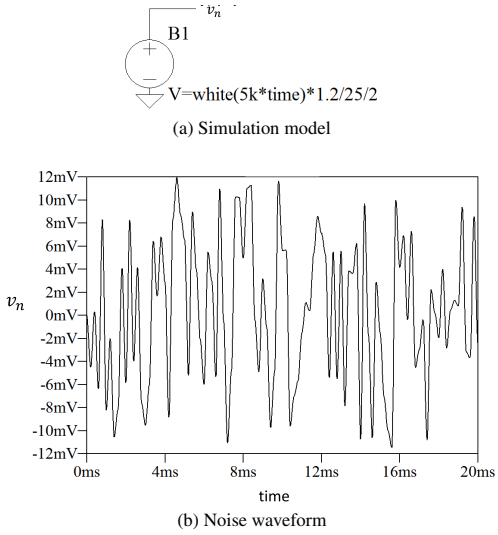
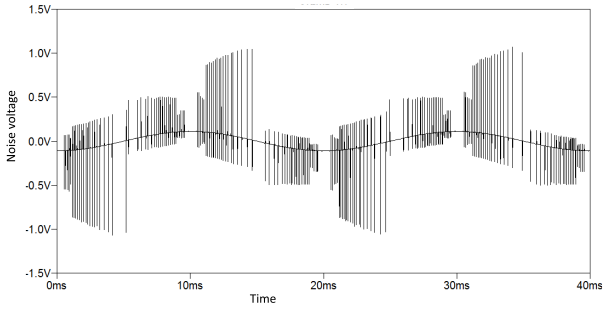


Fig. 9. Noise voltage waveform superpositioned on the reference voltage

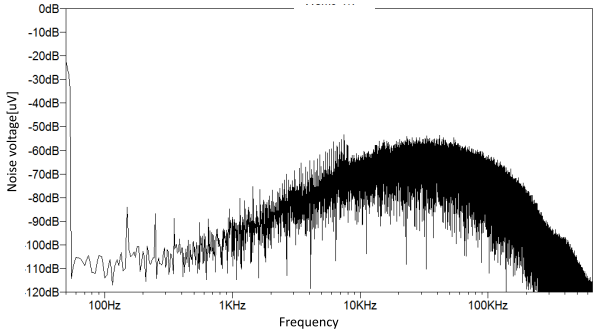
Table 6. Simulation results for Fig. 8 and regulatory limits

Category	Regulation	Frequency range	Limits	(1)Dual LED string		(1)+(2)Peak current limiter		(1)+(3)Noise superposition		(1)+(2)+(3)	
				Simulation	Margin	Simulation	Margin	Simulation	Margin	Simulation	Margin
Harmonic current emission	JIS C 6100-3-2	2nd harmonic	−34dBc	−40dBc	6dB	−40dBc	6dB	−38dBc	4dB	−41dBc	7dB
		3rd harmonic	$-(10.5\text{dBc} + 20\log_{10}\lambda)$[(a)]	−14dBc	3.5dB	−18dBc	7.5dB	−13dBc	2.5dB	−14dBc	2.6dB
		5th harmonic	−20dBc	−23dBc	3dB	−18dBc	-2dB	−22dBc	2dB	−22dBc	2dB
		7th harmonic	−23dBc	−27dBc	4dB	−30dBc	7dB	−27dBc	3dB	−33dBc	10dB
		9th harmonic	−26dBc	−29dBc	3dB	−29dBc	3dB	−29dBc	3dB	−29dBc	3dB
		11th to 39th harmonic	−30dBc	< −25dBc	< −3.5dB	< −25dBc	< −3.5dB	< −39dBc	> 9dB	< 40dB	> 10dB
Emission of radio frequency	CISPR15	9kHz～50kHz	110dBμV = −10dBV	< 78dBμV	> 32dB	< 77dBμV	> 33dB	< 71dBμV	> 39dB	< 66dBμV	> 44dB
		50kHz～150kHz	90~80dBμV[(b)]	< 78dBμV	> 2dB	< 76dBμV	> 4dB	< 69dBμV	> 11dB	< 73dBμV	> 7dB
		150kHz～500kHz	66~56dBμV[(b)]	< 71dBμV	< −15dB	< 61dBμV	< −5dB	< 55dBμV	> 1dB	< 50dBμV	> 10dB
		500kHz～5MHz	56dBμV	< 36dBμV	> 20dB	< 33dBμV	> 23dB	> 25dBμV	> 31dB	< 30dBμV	> 26dB
		5MHz～30MHz	60dBμV	< −6dBμV	> 54dB	< −6dBμV	> 54dB	< −6dBμV	> 54dB	< −7dBμV	> 67dB

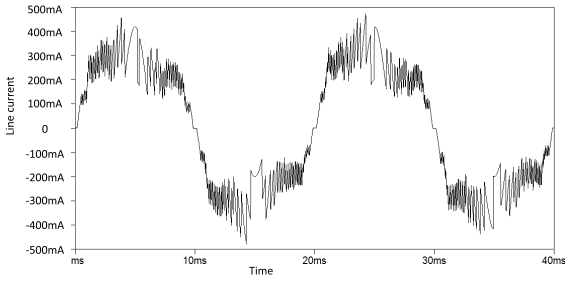
dBc: Ratio of the noise voltage to the line frequency component, (a) λ is assumed to be 0.9,
(b) The limit decreases linearly as the logarithmic value of frequency increases.



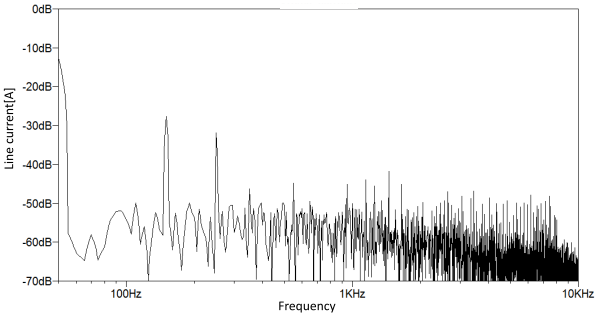
(a) Time domain line noise voltage



(b) Frequency domain line noise voltage



(c) Time domain line current



(d) Frequency domain line current

Fig. 10. Waveforms of simulation results

(3) on Table 6 indicate the numbers of the measures that are mentioned in the preceding paragraph. (1)+(2) refers to measures (1) and (2) being performed simultaneously. (1)+(3) refers to measures (1) and (3) being performed simultaneously. (1)+(2)+(3) refers to the three measures being performed. Out of the results on Table 6, the results (top portion) for the harmonic current regulation (JIS C 6100-3-2) can be directly compared to Table 5 as they are a carrier ratio. The results (bottom portion) for the radio interference regulation (CISPR15) are absolute levels. As Table 5 shows the results for LED string 1 (Fig. 3) and Table 6 shows the results for LED string 2 (Fig. 8), a difference of approximately 6 dB needs to be considered.

From the results of the (1)+(2)+(3) trial in the same table, it is clear than conducted emission standards can be satisfied with much more allowance, if the three measures are conducted, even in the absence of a reactor in the power line input unit. The wave form of the components in this case is shown in Fig. 10. Figures (a) and (b) are the time axis and the noise terminal voltage on the frequency axis, respectively. Terminal voltage is the voltage of both ends of R2 on the LISN. Figures (c) and (d) represent the power source line current.

4. Efficiency Analysis

4.1 Power Consumption Simulation Results

Table 7 shows the simulation results after application of the EMC measures ((1)+(2)+(3)) for electricity consumption, efficiency, power factor, and instantaneous maximum current.

An efficiency of 93% and a power factor of 96% is achieved while supplying a voltage used for an average LED apparatus (~24 W).

4.2 Analysis of Loss Table 8 shows the simulation results for the electric power loss for every component after the EMC measures. The loss in the shunt FET is due to the channel resistance. The loss due to gate resistance is included in the gate drive circuit loss. The loss of the peak current control circuit is the loss in M13, M23, R11, and R21. Figure 11 shows the values of Table 8 in a Pareto chart. The loss of the shunt FETs and the rectifier circuit make up approximately 80% of all losses.

Table 7. Simulation results of power consumption, after improvements

	Simulation result	Unit
Total power consumption, P_t	23.7	W
Power consumption in LEDs, P_{LED}	22.0	W
Peak current	460	mA
Power factor	0.960	
Efficiency	93.0	%

Table 8. Simulation results of losses, after improvements

	Value
Power loss in bypassing FETs	970mW
Power loss in gate drive circuits	132mW
Power loss in bridge rectifier	325mW
Power loss in peak current limiters	193mW

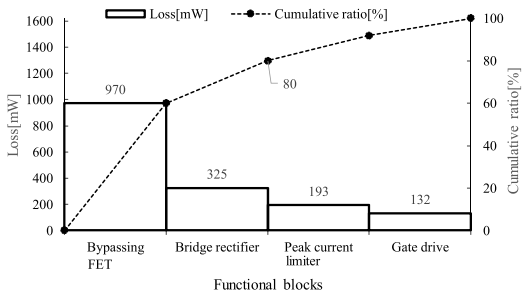


Fig. 11. Pareto chart of the losses

5. Summary

The simulation results demonstrate that the conceptual circuit via the LED switching format can achieve satisfactory efficiency and performance without using an electrolytic capacitor or a non-electrolytic capacitor. This conceptual circuit allows for lighting apparatus to be used for as long as the LED functions unlimited by the limitations of the electrolytic capacitor's lifespan.

In order to satisfy conducted emission regulations, the LED strings are setup in a dual format. Standard values can be satisfied by controlling the voltage range that lights up one LED string, adding noise to the reference voltage, which controls switching, and installing a peak current control circuit. In this case, an LED drive circuit can be made solely with a solid-state semiconductor and a resistor element without the need to insert a reactor element into the power input. This suggests that this conceptual format can produce practical circuits that are long-lasting. Hereafter, the researchers intend to use a prototype in order to further understand issues that may arise upon implementation.

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Kenji Yamamoto (Member) was born in 1956. He received his B.E. degree in electrical engineering from Shibaura Institute of Technology in 1980, M.E. in electronic engineering from Sophia University in 1982, and Ph.D. from the University of Electro-Communications in 2015. He worked for Hewlett-Packard Co. for twenty-six years and joined Human Resources Development Polytechnic University as a researcher for four years. He has been appointed as an associate professor at Shizuoka Institute of Science and Technology. His interest is in analog integrated circuit design, tactile reproduction, motor control theory.

Richard Lum (Non-member) has a Bachelor of Engineering degree with 1st Class Honours from the National University of Singapore (NUS) and an MBA with the UK Open University. Currently, he is an independent design consultant. He has several patents related to Optical Isolation and Power Circuits. He is a Senior Member of the IEEE.

Hisashi Takahashi (Senior Member) was received his B.E. from Human Resources Development Polytechnic University in 1975. He worked at the university after his graduation as a research assistant, a lecturer, and was appointed as an associate professor. He is a Ph.D. in engineering. From Oct. 1997 to Nov. 1999, he was sent to Tianjin University of Technology and Education, China as an expert in control systems. He has been appointed as a professor at Shizuoka Institute of Science and Technology from 2011. His interest is in control systems for small motors, parameter estimation for motor control systems, systems for assisting a disabled person. He is a member of IEEE, The Japan Society for Precision Engineering, The Society of Instrument and Control Engineers, and The Robotics Society of Japan.