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Paper
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Design Approach of Non-Isolated Converters with Passive Soft Switching

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High-frequency switching techniques enable the miniaturization of inductors in non-isolated DC/DC converters. However, higher frequency converters cause large switching power losses. This paper proposes a design method for a high-frequency, non-isolated buck DC/DC converter with a passive soft-switching circuit. The calculation results of the converter revealed decrease in power losses compared to that of a hard switching converter, for over 50 kHz. A 2.1 kW prototype was designed for reification, and it achieved a power efficiency of 95.6%.

Keywords: non-isolated DC/DC, soft switching, DC/DC converter, high-frequency switching

1. Introduction

In recent years, there has been high demand for power converters with increased power density [(1)(2)]. In order to create power converters that are small, lightweight, and high-power, it is necessary to use low-loss (high efficiency) circuit architectures. In non-isolated DC/DC converters, the use of high frequencies allows the transformer, which is normally a large part, to be made smaller. However, one issue in using high frequencies is that switching losses become concentrated at the switching element. In order to develop circuits with low losses at the switching element, researchers have studied a wide variety of soft switching circuit topologies [(3)–(6)]. In particular, the passive soft switching method [(7)–(12)], which uses the phenomenon of resonance, does not require additional switching elements and is compatible with high-frequency operation. Therefore, the authors have investigated passive soft-switching buck converters (PSW-BC) that include inverters, capacitors, and diodes for resonance [(13)]. In PSW-BC, by selecting parameters for the additional passive components based on the operating power specifications, it possible to perform soft switching of the switching element. In this paper, we estimated power losses for the case of a unidirectional buck circuit with an input of 48 V and an output of 14 V–150 A (2.1 kW) with a PSW-BC. The estimates showed that this method reduces losses compared to the buck chopper method in the frequency range above 50 kHz. In this paper, we describe the principle of operation and our design method for the PSW-BC. We also discuss results regarding estimated losses which we obtained based on the principle of operation, and results regarding efficiency measurements which were taken using a prototype.

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2. Circuit Architecture and Principle of Operation

2.1 PSW-BC Circuit Architecture Figure 1 shows the circuit architecture of the PSW-BC. The PSW-BC consists of several elements that already exist in buck choppers, including smoothing capacitors Cin and Cout, smoothing inductor L1, and switching elements S1 and S2, as well as additional resonance capacitors C1 and C2, resonance inductor L2, and diodes D1–D4. The PSW-BC is a non-isolated buck converter that transmits power in one direction from the power source to the load. The circuit specifications are shown in Table 1. We chose the power supply voltage (V_{in}) at the input side to be 48 V, the voltage applied to the load (Vout) to be 14 V, and the current through the load to be within the

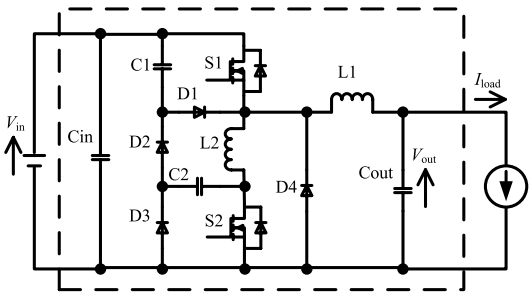


Fig. 1. The circuit diagram of PSW-BC

Table 1. Operating specification

input voltage	V_{in}	48 V
output voltage	V_{out}	14 V
load current	I_{load}	150 A
inductance of L1	L_1	6 uH
inductance of L2	L_2	70 nH
capacitance of C1	C_1	110 nF
capacitance of C2	C_2	330 nF
forward voltage of body diode	V_{diode}	0.8 V
forward voltage of D1~D4	V_D	0.87 V

range of 0–150 A, resulting in a maximum output power of 2.1 kW. In addition, the constants for each of the components listed in Table 1 were chosen in order to be able to implement soft switching under the above power specifications. We will describe our method for selecting these constants later.

The gate signals (G1, G2) of S1 and S2 use complementary switching. As for the dead-time between when G1 turns OFF and G2 turns ON (t_{d1}) and the dead-time between when G2 turns OFF and G1 turns on (t_{d2}), t_{d1} is chosen in order to satisfy the design requirements described in Section 2.4. Furthermore, even though it is still possible to achieve soft switching operation if a diode is used for S2, synchronous rectification is used in order to reduce losses.

Control of the PSW-BC is performed by detecting the voltage V_{out} across the conductor and using voltage feedback control in order to maintain the voltage applied to the load at a constant level. The ideal value for OnDuty (D_{on}) of the switching element S1 is the same as for the chopper circuit, or $D_{on} = V_{out}/V_{in}$.

2.2 Soft Switching Principle of Operating Figure 2 shows a total of nine states (State 1–9) of the PSW-BC which are categorized according to different current circuits. Figure 3 shows the current and voltage waveforms for each component. The solid-line arrows in Fig. 2 indicate the paths through which the main currents flow, and the dotted-line arrows indicate the paths through which the resonant currents and auxiliary currents flow.

The soft switching operation consists of ZCS-type soft switching, in which L2 limits the rate of change in the current when S1 turns on, and ZVS-type soft switching, in which C1, which is placed in parallel, is charged and limits the rate of change in the current when S1 turns off. Therefore, the ability of soft switching to reduce losses depends on the constants L_2 and C_1.

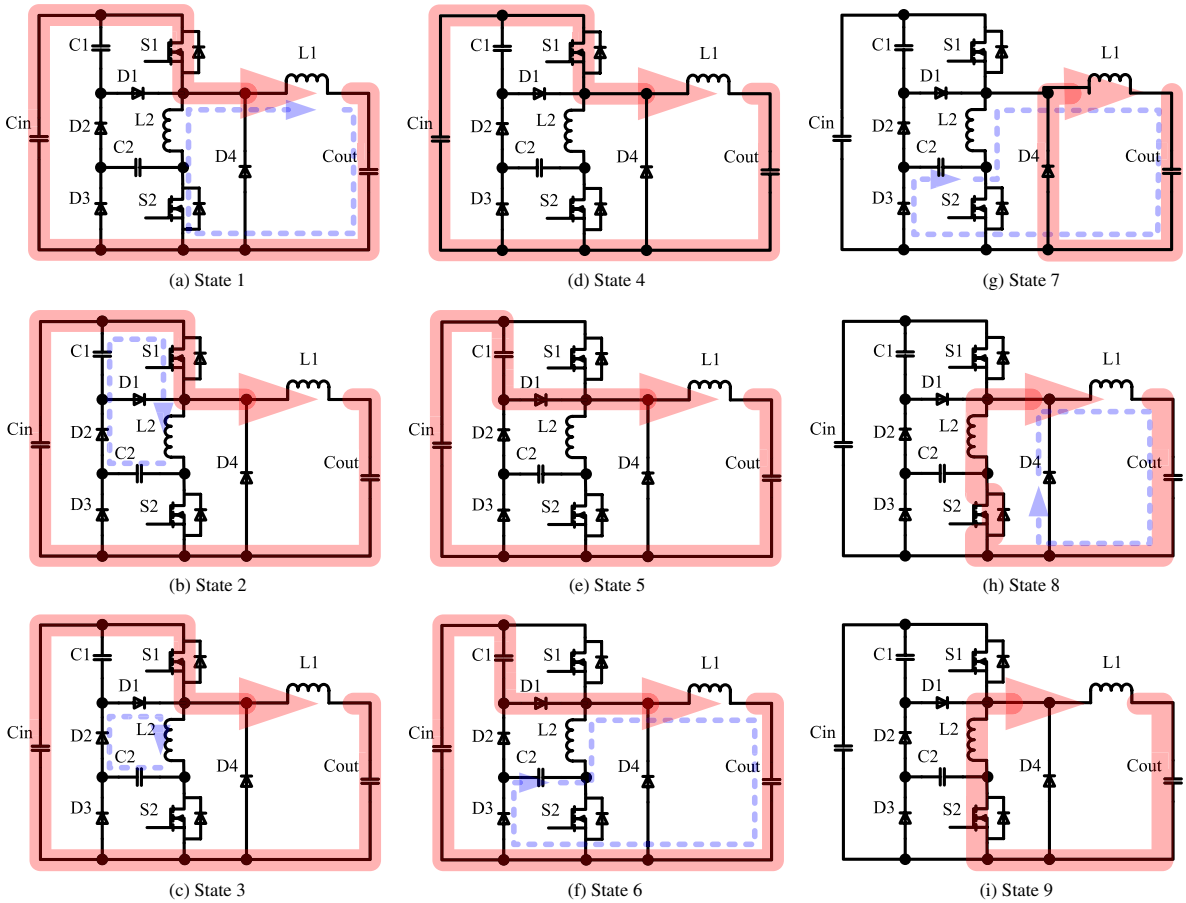
Next, we explain the operation during State 1–9. In addition, we include the equations that are important for describing the soft switching operation, including the current and voltage for each state as well as their rates of change and resonance frequencies. Here, let I_r represent the ripple current of L1.

(1) State 1: $t_0 - t_1$ (Refer to Fig. 2(a), Fig. 3)
(Path 1) Cin → S1 → L1 → Cout → Cin
(Path 2) S2 → L2 → L1 → Cout → S2

State 1 begins when S1 turns on (t_0). The DS voltage of S1 becomes zero after the rise-time (t_r) has elapsed, but the current through path 2 approaches zero gradually due to the voltage applied to L2. Here, the voltage applied to L2 is $V_{in} + V_{diode}$, and the rate of change in current is given by Equation (1).

$$\frac{dI_{L2}}{dt} = \frac{V_{\text{in}} + V_{\text{diode}}}{L_2} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

When the rate of change of current is sufficiently large compared to the rate of change of voltage when S1 turns on in Equation (1), there is no overlap between the current and voltage in the S1 waveform (t_0), as shown in Fig. 3, and the turn-on loss of S1 is almost zero. t_{s1} is defined as the period of time until t_1, which is the instant when the current through



(a) State 1 (d) State 4 (g) State 7
(b) State 2 (e) State 5 (h) State 8
(c) State 3 (f) State 6 (i) State 9

Fig. 2. Current pathway of each state

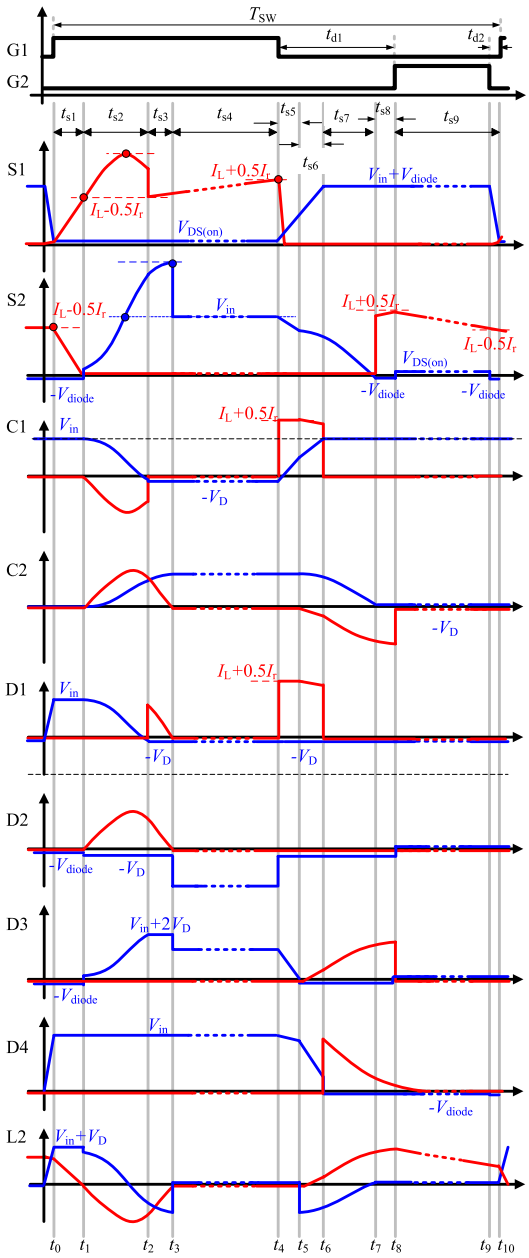


Fig. 3. Ideal voltage and current waveform of each device for PSW-BC circuit from State 1 to State 9. $V_{DS(on)}$ is drain-source voltage of S1 and S2, t_{d1} and t_{d2} are dead-times between G1 and G2, and T_{sw} is switching cycle

path 1 reaches $(I_L - I_r/2)$.

(2) State 2: $t_1 - t_2$ (Refer to Fig. 2(b), Fig. 3)
(Path 1) Cin → S1 → L1 → Cout → Cin
(Path 2) C1 → S1 → L2 → C2 → D2 → C1

State 2 begins at t_1. A resonance current flows through the CLC circuit of path 2 with C1 as the energy source. Current only flows in the forward direction due to diode D2, and the voltage across C1 reaches zero. t_{s2} is defined as the period until this instant, t_2. The resonance frequency of the CLC circuit at this time is given by Equation (2), and the CLC resonance current is given by Equation (3).

$$\omega_0 = \sqrt{\frac{1}{L_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)} \cdots\cdots (2)$$

$$I_{CLC}(t) = \frac{\omega_0 (V_{in} - V_D)}{\dfrac{1}{C_1}+\dfrac{1}{C_2}} \sin(\omega_0 t) \cdots\cdots (3)$$

Since the maximum current that flows through S1 is determined by the maximum value of the resonance current in Equation (3), the values that are chosen for constants C1, C2, and L2 are important in the design of S1. Details are described in Section 2.4.

(3) State 3: $t_2 - t_3$ (Refer to Fig. 2(c), Fig. 3)
(Path 1) Cin → S1 → L1 → Cout → Cin
(Path 2) L2 → C2 → D2 → D1 → L2

State 3 begins at t_2. A resonance current flows through the LC circuit formed by path 2 due to the energy stored in L2. Current only flows in the forward direction due to diode D1 and D2, similar to State 2. t_{s3} is defined as the period until t_3, which is the instant when the current through the inductor becomes zero. The resonance frequency of the LC circuit is given by Equation (4).

$$\omega_1 = \sqrt{\frac{1}{L_2 C_2}} \cdots\cdots (4)$$

The energy that was charged in C1 has been transferred to C2 after the periods for State 2 and State 3 have elapsed. The voltage applied to C2 after CLC/LC resonance has finished is given by Equation (5).

$$V_{C2} = \frac{C_1}{C_2} V_{in} \cdots\cdots (5)$$

Since the voltage applied to S2 is determined by the voltage applied to C2 in Equation (5), the values that are chosen for constants C1and C2 are important in the design of S1. Details are described in Section 2.4

(4) State 4: $t_3 - t_4$ (Refer to Fig. 2(d), Fig. 3)
(Path 1) Cin → S1 → L1 → Cout → Cin

State 4 begins at t_3. State 4 corresponds to the period until the instant when S1 turns off (t_4) and is proportional to the time that S1 is on $(D_{on}T_{SW})$. This period is defined as t_{s4}.

(5) State 5: $t_4 - t_5$ (Refer to Fig. 2(e), Fig. 3)
(Path 1) Cin → C1 → D1 → L1 → Cout → Cin

State 5 begins when S1 turns off (t_4). The current through S1 becomes zero after the rise-time (t_f) has elapsed. Since path 2 charges C1 through D1, the voltage across C1 is given by Equation (6) assuming that the output capacity (C_{OSS}) of the switching element is sufficiently small compared to C1 and can be ignored.

$$\frac{dV_{S1}}{dt} = \frac{1}{C_1}\left(I_L + \frac{I_r}{2}\right) \cdots\cdots (6)$$

If the rate of change of the voltage in Equation (6) is sufficiently large compared to the rate of change of current when S1 turns off, there will be no overlap between the current and the voltage waveforms, as shown in Fig. 3 for the S1 waveform (t_4), resulting in the turn-off losses for S1 becoming almost zero.

The decrease in the voltage applied to D3 that accompanies the rises in V_{S1} and V_{C1} causes D3 to turn on. t_{s5} is defined as the period until t_5, the instant when D3 turns on.

(6) State 6: $t_5 - t_6$ (Refer to Fig. 2(f), Fig. 3)
(Path 1) Cin → C1 → L1 → Cout → Cin

(Path 2) C2 → L2 → L1 → Cout → D3 → C2

State 6 begins at t_5. In addition to path 1 in State 5, resonance current with a frequency of ω_1 flows through D3 and discharges C2. A current that is equivalent to the current term on the right side of Equation (6) minus the resonance current flows through path 1 and continues until V_{S1} reaches V_{in}. t_{s6} is defined as the period until t_6, the instant when the current through path 1 becomes zero.

(7) State 7: $t_6 - t_7$ (Refer to Fig. 2(g), Fig. 3)

(Path 1) D4 → L1 → Cout → D4

(Path 2) C2 → L2 → L1 → Cout → D3 → C2

State 7 begins at t_6. A current that is equivalent to current L1 minus the current through path 2 flows through path 1. t_{s7} is defined as the period until t_7, the instant when voltage across C2 becomes zero.

(8) State 8: $t_7 - t_8$ (Refer to Fig. 2(h), Fig. 3)

(Path 1) S2 → L2 → L1 → Cout → S2

(Path 2) D4 → L1 → Cout → D4

State 8 begins at t_7. t_{s8} is defined as the period until t_8, the instant when S2 turns on.

(9) State 9: $t_8 - t_{10}$ (Refer to Fig. 2(i), Fig. 3)

(Path 1) S2 → L2 → L1 → Cout → S2

State 9 begins at t_8. t_{s9} is defined as the period until t_{10}, the instant when S2 turns on. Although current continuous to flow through the path through D4, the current converges to a value that is sufficiently small due to the resistance ratio when S2 is on, so this current can be ignored when estimating losses.

Up until now, we explained the principle of operation assuming that the inductor current, including the ripple, is greater than zero. However, soft switching operation is not possible when the inductor current crosses zero and becomes negative (backward operation). In this paper, we have chosen a value for the inductance of L1 such that soft switching is possible under the rated load (V_{in} = 48 V, V_{out} = 14 V, I_{load} = 150 A (2.1 kW)).

Considering the conditions that are required for soft switching operation as described above, we derived equations for calculating periods $t_{s1} - t_{s9}$ of State 1–9 for the PSW-BC based on the principles of operation and Equations (1)–(6), and calculated the results using the constants in Table 1. The results are shown in Table 2. Here, a two-phase interleaved operation PSW-BC was selected in order to make the prototype small. I_{load} is twice as large as the average current I_L of L1 in Table 2.

In order to verify the validity of the equations shown in Table 2, we used a circuit simulator package (PSIM) created by Powersim Software to conduct a simulation of the operation. A comparison of the results obtained from the simulation waveforms and the calculation results shows that the error for t_{s5} and t_{s6}, which are relatively short, was approximately 20%, and that the error for the other periods was approximately 7%. Therefore, we determined that we were able to successfully formulate equations that describe the operation of the PSW-BC. In the next section, we analyze losses in the PSW-BC by creating estimates.

2.3 Conditions for Soft Switching In the following estimates for losses in the PSW-BC, we assume that the switching loss is zero due to the use of soft switching. However, in order to approximate losses as zero, it is necessary

Table 2. Comparison of period from calculation results for each state distance with that from simulation results of PSIM

	Calculating formula	Calculate [ns]	PSIM [ns]
t_{s1}	$\frac{(I_L - I_r/2)L_2}{V_{in} + V_{diode}}$	82	80
t_{s2}	$\frac{1}{\omega_0}\cos^{-1}\left(\frac{C_1 + C_2}{C_2}\frac{V_{in}}{V_D - V_{in}} + 1\right)$	147	150
t_{s3}	$\frac{1}{\omega_1}\tan^{-1}\left(\frac{\beta}{C_2\omega_1}\cdot\frac{1}{\alpha + 2V_D}\right)$	136	130
t_{s4}	$D_{on}T_{sw} - (t_{s1} + t_{s2} + t_{s3})$	5469	5390
t_{s5}	$C_1\frac{(V_{in} - V_D - V_{C2}(t_{s3}))}{I_L + I_r/2}$	25	20
t_{s6}	$C_1\frac{(V_D + V_{C2}(t_{s3}))}{I_L + I_r/2}$	33	40
t_{s7}	$\frac{\pi}{2\omega_1} - C_1\frac{(V_D + V_{C2}(t_{s3}))}{I_L + I_r/2}$	206	220
t_{s8}	$T_{d1} - (t_{s5} + t_{s6} + t_{s7})$	236	220
t_{s9}	$(1 - D_{on})T_{sw} - T_{d1}$	13666	13750

where

$$\alpha = (V_{in} - V_D)\left[\frac{C_1}{C_1 + C_2}(1 - \cos\omega_0 t_{s2})\right],$$

$$\beta = \frac{C_1C_2}{C_1 + C_2}\omega_0 (V_{in} - V_D)\left[\frac{C_1}{C_1 + C_2}\sin\omega_0 t_{s2}\right],$$

$$V_{C2}(t_{s3}) = \frac{\alpha + 2V_D}{\cos\omega_1 t_{s3}} - 2V_D.$$

for the following conditions (1)–(4) to be satisfied.

(1) In order to obtain the desired switching loss reduction when S1 turns on, the length of State 1, t_{s1}, must be sufficiently long compared to the rise- time of S1 (t_r). Since t_{s1} is proportional to L_2 in the equation for t_{s1} in Table 2, Equation (7) holds. Larger values of L_2 are better for soft switching, but since the reduction effect converges to zero anyway, we chose a value for L_2 to satisfy other conditions and obtain sufficient switching loss reduction.

$$t_r \ll t_{s1} \propto L_2 \cdots\cdots (7)$$

(2) In order to obtain the desired switching loss reduction when S1 turns off, the length of State 5 and State 6, $t_{s5} + t_{s6}$, must be sufficiently long compared to the rise-time of S1 (t_f). Since $t_{s5} + t_{s6}$ is proportional to C_1 in the equations for t_{s5} and t_{s6} in Table 2, Equation (8) holds. Larger values of C_1 are better for soft switching, but since the reduction effect converges to zero anyway, we chose a value for C_1 to satisfy other conditions and obtain sufficient switching loss reduction.

$$t_f \ll t_{s5} + t_{s6} \propto C_1 \cdots\cdots (8)$$

(3) In order for the energy charged in C1 to transfer to C2 and make the voltage across C1 become zero, the total length of Stage 1, State 2, and State 3 must be shorter than the length of time that S1 is on ($D_{ON}T_{SW}$). Therefore, in order for it to be possible to use soft switching for turning off S1, Equation (9) must hold.

$$D_{on}T_{SW} \geq t_{s1} + t_{s2} + t_{s3} \cdots\cdots (9)$$

Based on Equation (9), it is difficult to select values for the capacitance of C1 and C2 and inductance of L2 for PSW-BC converters with low buck ratios.

(4) In order to use the CLC resonance and discharge C1 until its voltage becomes zero, the CLC resonance current must always be greater than zero. Therefore, Equation (10) holds.

$$C_2 \geq C_1 \cdots\cdots (10)$$

2.4 Design Requirements for Components In addition to the above conditions for soft switching, it is necessary for the following conditions (1)–(3) to be satisfied from the perspective of component tolerance.

(1) The current that flows through S1 during t_{s2} is the sum of the current through L1 and the resonance current. The circuit should be designed so that current through S1 is under the rated current (I_{S1-max}). The maximum CLC resonance current depends on the values of the inductance of L1 and the capacitances of C1 and C2, as shown in Equation (11). Therefore, this defines the maximum values for C_1 and C_2.

$$I_{\mathrm{S1-max}} \geq I_{\mathrm{L}} - \frac{I_{\mathrm{r}}}{2} + \sqrt{\frac{C_1 C_2}{L_2 (C_1 + C_2)}} (V_{\mathrm{in}} - V_{\mathrm{D}}) \cdots\cdots (11)$$

(2) The voltage that is applied to S2 during t_{s2} is the sum of the input voltage and the voltage applied by C2. The circuit should be designed so that voltage that is applied to S2 is under the rated voltage (V_{S2-max}). The maximum voltage that is applied to S2 depends on the value of the values of the capacitances of C1 and C2, as shown in Equation (12). Therefore, this defines the relationship between the maximum value for C_1 and C_2.

$$V_{\mathrm{S2-max}} \geq V_{\mathrm{in}} + \sqrt{\frac{C_1}{C_2}} (V_{\mathrm{in}} - V_{\mathrm{D}}) \cdots\cdots (12)$$

(3) If S2 turns on before C2 has completely discharged, a short-circuit current will flow through the path through C2 → S2 → D3 → C2, resulting in enormous losses. Therefore, the dead-time (t_{d1}) is chosen according to Equation (13).

$$t_{\mathrm{s5}} + t_{\mathrm{s6}} \leq t_{\mathrm{d1}} \leq \frac{1}{2} (1 - D_{\mathrm{on}}) T_{\mathrm{SW}} \cdots\cdots (13)$$

The constants for the elements shown in Table 1 were chosen to satisfy all of the conditions in (7)–(13).

3. Prototype Test

We created a prototype of a non-isolated buck DC/DC converter using a PSW-BC, validated its soft switching operation, and compared its losses with the theoretical losses.

3.1 Consideration of Frequency Figure 4 shows estimates of the losses in the switching part (C1, C2, L2, S1, S1, S2, and D1–D4) and a comparison with results from the chopper method (hard switching). The constants for the components were chosen as shown in Table 1 in order to satisfy the conditions in Equations (7)–(13). The switching losses for S1 and S2 in the PSW-BC are assumed to be zero.

MOSFETs from the same series manufactured by Infineon were used for the PSW-BC and chopper method. However, since the breakdowns of the switching losses and the conductance losses in each of these methods are different, we chose different MOSFETs that are suitable for each method. In particular, for the PSW-BC, we selected a component with low resistance during the ON state since the PSW-BC has no switching losses (manufactured by Infineon, IPB180N10S4-02, $R_{DS(on)}$: 2.5 mΩ, Q_g: 156 nC, three in parallel), and for the chopper method, we selected an element with a good balance between the gate load, which is proportional to the switching loss, and the resistance during the ON state (manufactured by Infineon, IPB100N10S3-05, $R_{DS(on)}$: 4.8 mΩ, Q_g: 135 nC, three in parallel) (since the switching losses of S1 are dominant at 50 kHz and 100 kHz as shown in Fig. 4(a), the total losses would be even larger if we had used IPB180N10S4-02 for the chopper method). Here, we assumed that the low-side of the chopper method circuit incurs only conductive losses since it uses synchronous rectification, and we derived Equation (14) for the switching losses for the high-side.

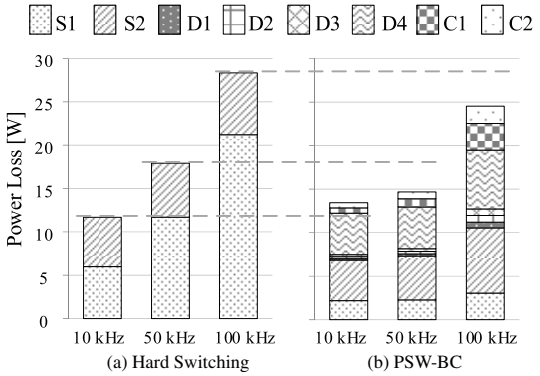


Fig. 4. Comparison result of switching and snubber devices of PSW-BC with hard switching devices

$$P_{\mathrm{SW\_H}} = \frac{1}{2} \times V_{\mathrm{in}} \times V_{\mathrm{out}} \times (t_{\mathrm{r}} - t_{\mathrm{f}}) \times f_{\mathrm{SW}} \cdots\cdots (14)$$

In addition, it is sufficient for L_2, which determines the resonance frequency, to have an extremely small value of 70 nH. In the prototype, L_2 is composed of wiring (bus bar), and the losses of L2 are ignored in the loss estimates in Fig. 4. The losses for capacitors C1 and C2 were derived by calculating the root mean squared values of the currents flowing through the capacitors (I_{C_RMS}) based on the principles of operation described in Section 2 and calculating $(I_{C\_RMS})^2 \times ESR$ (f = 50 kHz) from the equivalent series resistance (ESR) of each component.

Comparing the rates at which the total losses increase with respect to the frequency for the chopper method and the PSW-BC in Fig. 4, it can be seen that the rate of increase for the PSW-BC is low, and that the total losses are expected to be lower than in the chopper method for the frequency region above 50 kHz. As described in Section 1, the purpose of using soft switching in this research is to mitigate the concentration of losses at the switching element accompanying high frequency operation. Examining the losses at S1 and S2 reveals that above 10 kHz, the losses are smaller than in the chopper method, and that above 50 kHz, the total losses, including the additional elements needed for soft switching, are expected to become lower. In the prototype tests, we operated the circuits using frequencies of 50 kHz and 100 kHz.

3.2 Validation of Soft Switching Operation

Figure 5 shows a photograph of the PSW-BC non-isolated

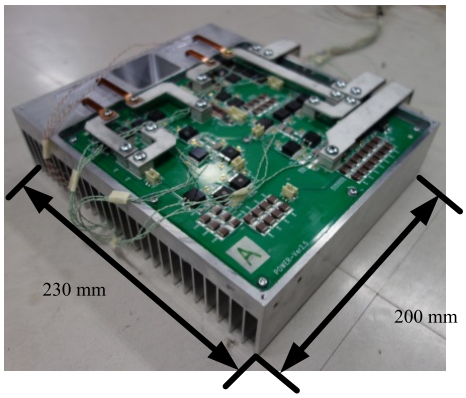


Fig. 5. The overview of the prototype of PSW-BC

buck converter. In addition to the components for the PSW-BC, the device includes shunt resistors for detecting current and switching elements for protection.

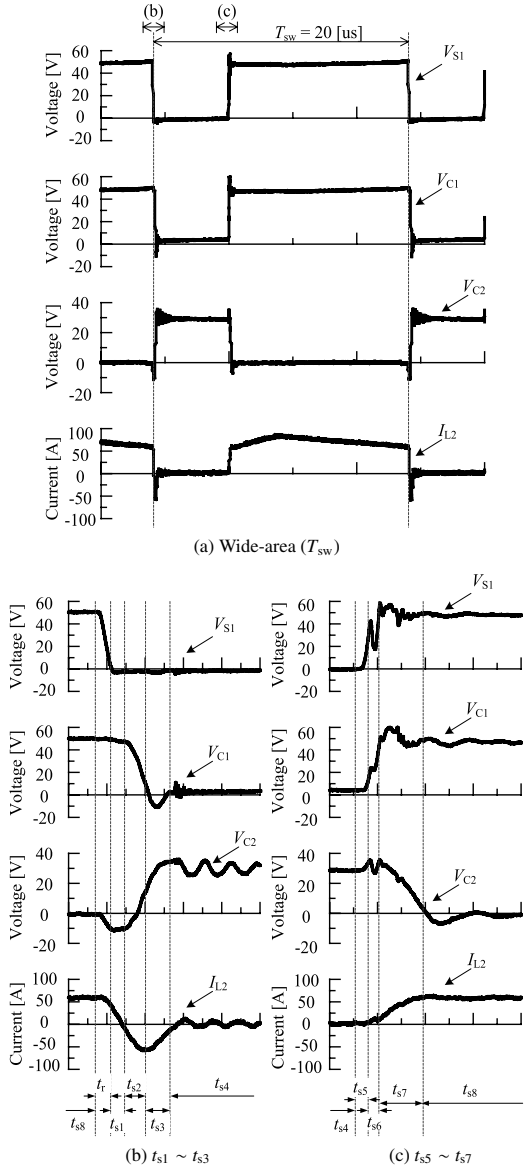
Figure 6(a) shows the measured waveforms for the drain-source voltage of S1, the voltage across C1, the voltage across C2, and the current through L2 for a frequency of 50 kHz. The measured waveforms are indicated in order as V_{S1}, V_{C1}, V_{C2}, and I_{L2}. Figure 6(b) and (c) show magnified views of the waveforms during the period when S1 is turned on ($t_{s1} - t_{s3}$) and when S1 is turned off ($t_{s5} - t_{s7}$).

Based on the waveform for the period during which S1 is turned on shown in Fig. 6(b), we verified that the resonance current flows through C1-L2-C2 between when the S1 voltage falls and period t_{s1} and that the voltage across C2 rises, which indicates that energy was transferred from C1 to C2. On the other hand, we observed that the voltage across C1 and the voltage across C2 behave differently from the ideal conditions shown in Fig. 3, in which they both become negative temporarily. Furthermore, we also observed that the voltage across S1 initially spikes when it rises, as shown in the waveform for the period during which S1 is turned off in Fig. 6(c).

The waveforms described above can be observed in PSIM as well by adding inductance components of only several 10 nH to the resonance current path. We surmise that this is due to parasitic elements. This demonstrates that it is necessary for circuit designers to thoroughly consider the circuit constants and parasitic elements when designing PSW-BC.

3.3 Loss Measurement Results Figure 7 shows a comparison of actual measurements of the loss (experiment) and estimates of the loss (calculation) from Fig. 4(b) for one phase of the prototype. Here, other than the value of the inductance of L2, the circuit design has no impact on soft switching operation. However, both the prototype and the model used for the estimates use an inductor that is composed of seven turns of a flat wire wound around a powder E-core. The estimated losses increase at low frequencies due to the copper losses of the inductor. The power measurements were conducted using the WT1800 power analyzer manufactured by Yokogawa Electric Corporation, and the input and output currents were measured by converting current to voltage using the CT200 manufactured by Yokogawa Electric Corporation.

The results for the actual measured losses (experiment)



The times of state obtained from waveform are t_{s1} = 75 ns, t_{s2} = 114 ns, t_{s3} = 128 ns, t_{s5} = 35 ns, t_{s6} = 42 ns and t_{s7} = 197 ns.

Fig. 6. Experimental waveform of prototype

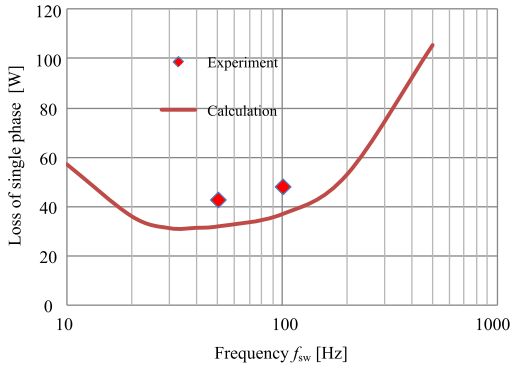


Fig. 7. Loss comparison on single phase PSW-BC of experiment with calculation (V_{in} = 48 V)

were approximately 10 W larger than the estimated losses (calculation) due to the effects of the waveforms due to the parasitic elements as explained in the previous section. However, we confirmed that the conversion efficiency was still

high at 95.6% for the maximum rated power of 2.1 kW (I_{load} = 150 A).

4. Conclusions

In this paper, we explained the principle of operation and a design method for the PSW-BC, which is a high-frequency non-isolated buck DC/DC converter that uses a soft switching method. In addition, we showed equations for calculating the lengths of time for all 9 states of the PSW-BC, and proved the validity of the equations through a comparison with simulation results. Furthermore, we estimated the losses based on the equations for calculating the lengths for each of the states, and showed operating frequencies for which the PSW-BC has lower losses than the chopper method.

Based on the above investigations, we created a prototype with an input voltage of 48 V, output voltage of 14 V, and rated current load of 150 A. The prototype achieved an efficiency of 95.6% at its maximum power conversion. However, the efficiency was approximately 1.4 points lower than the estimated efficiency due to the effect of parasitic elements. In the future, it is necessary to consider the parasitic elements and improve the circuit configuration and selection of constants.

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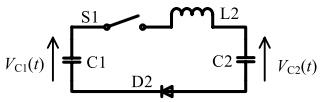
Appendix

Process for Deriving Equation (3)

Drawing only the CLC resonance path yields the following diagram.



The initial conditions when CLC resonance begins are as follows.

$$\begin{cases} V_{C1}(t_1) = V_{in} \\ V_{C2}(t_1) = 0 \\ I_{CLC}(t_1) = 0 \end{cases}$$

Kirchhoff's circuit laws for the current and voltage during period t_{s1} are written as follows.

$$\begin{cases} L_2 \dfrac{dI_{CLC}(t)}{dt} = V_{C1}(t) - V_{C2}(t) - V_D \\ C_1 \dfrac{dV_{C1}(t)}{dt} = -C_2 \dfrac{dV_{C2}(t)}{dt} = -I_{CLC}(t) \end{cases}$$

Solving the above equations for $I_{CLC}(t)$ gives Equation (3).

Process for Deriving Equation (3)

From Equation (3), the maximum value of $I_{CLC}(t)$ is as follows.

$$I_{CLC(max)} = \frac{\omega_0(V_{in} - V_D)}{\dfrac{1}{C_1} + \dfrac{1}{C_2}}$$

Equation (11) is derived from the above equation along with the current flowing through L1.

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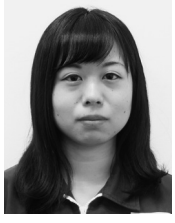

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