

Secondary-side-only Phase-shifting Voltage Stabilization Control with a Single Converter for WPT Systems with Constant Power Load

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(Manuscript received Jan. 31, 2018, revised June 28, 2018)

In recent years, wireless power transfer technology has received considerable attention because of its wide range of applications. Most of the literature focuses on the resistance load or constant voltage load, and the constant power load is almost never considered. The open loop transfer function of a constant power load is unstable, and therefore closed loop stabilization is required. Furthermore, communication between the two sides is often used but it may not be available. In order to stabilize the load voltage without resorting to coordination with the primary side and discontinuous operation causing big voltage transients, this paper proposes a control strategy for only the secondary side using a single converter. It is based on the combination of synchronous rectification and symmetric phase shift, without communication with the primary side. While the primary side is not manipulated, the AC/DC converter regulates the amplitude of the secondary coil voltage and stabilizes the constant power load voltage on the DC side via a simple PI control. In this paper, the control concept, design and stability analysis are provided. The proposed control is verified through experimental results in both static and dynamic scenarios, achieving a controller that is simple to design and has smooth waveforms.

Keywords: wireless power transfer, power control, constant power load, secondary side, phase shifting

1. Introduction

Wireless power transfer (WPT) technology recently has become appealing for both industrial and automotive applications because it simplifies the powering process and eliminates potential dangers for the user. WPT by magnetic resonant coupling achieves high efficiency and is capable of transmitting high power⁽¹⁾. There are different types of WPT tuning by magnetic resonant coupling, depending on the circuit topology⁽²⁾: in particular, the series-series (SS) compensation allows high power to flow on the secondary side with high efficiency. These characteristics are favorable for applications such as Electric Vehicles (EVs). Literature involving WPT for EVs is abundant^{(2)–(7)}. Currently, static WPT is on a quite mature state and is ready to be launched on the market; on the other hand, practical in-motion WPT is still under research. While static WPT is not so different from plug-in EV charging, in-motion WPT can reduce both battery weight and range anxiety, thus mitigating the burden of the EV user, who can finally drive without thinking too much about the position of charging station; some prototypes have achieved good results^{(8)–(11)}.

Most of previous studies concentrated on coil design, compensation topologies and system parameters. However, simply being able to transfer power to the load without using cables is not sufficient to achieve an optimized performance. Control is an important part of the design and can remarkably change the requirements for converters; it depends strongly on the number of converters available and the requirements of the load. Usually, control is performed in order to maximize the transmitting efficiency^{(12)–(14)}. Tracking and control of maximum efficiency point can be performed from primary side⁽¹⁵⁾ or by secondary side⁽¹⁶⁾. However, also power control is important in order to meet the load requirements: in this case, it is advisable to perform it by the secondary side of the system⁽¹⁴⁾⁽¹⁷⁾. Communication with the primary side may be used but it is not strictly necessary, thus the development of controls not relying on communications is advantageous in terms of system cost and avoidance of communication delay problems. For instance, some researches have proposed power and efficiency control performed only in the secondary side⁽¹⁸⁾⁽¹⁹⁾ by using two active converters instead of the typical combination of full diode bridge rectifier and DC/DC converter. However, depending on the application, having two converters on the secondary side may be impossible due to space and cost limitations.

Concentrating the control on the secondary side of a WPT system allows to better tailor the control to the load. In past research, the load has almost always been a resistance⁽²⁰⁾⁽²¹⁾ or a constant voltage load such as a battery or similar storage system⁽¹⁶⁾⁽¹⁷⁾⁽²²⁾⁽²³⁾. However, there are also other applications such as motors that are constant power loads (CPL). While

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research about CPL has been performed for other application such as distributed grids regulation or automotive⁽²⁴⁾, in WPT application it is very seldom considered. Some basic studies about switching regulators⁽²⁵⁾, industrial stages⁽²⁶⁾ and DC motors⁽²⁷⁾ have been reported. Some research about control of motors of EV have also been carried out^{(28)–(31)}. While in^{(28)–(29)} there is no detail on the control method, in⁽³⁰⁾ and⁽³¹⁾ a control based on both sides is performed. In particular, the information on the load torque and voltage are transmitted to the primary side by Bluetooth signal, and the primary side chopper regulates the battery voltage in order to match the load voltage reference. Moreover, the problem of CPLs is that they have negative dynamic resistance characteristic ($dV/dI < 0$). It means that if the voltage increases, the current decreases and viceversa: this behaviour becomes a loop and leads to instability of the system. It is then necessary to control either the voltage or the current in order to guarantee system stability. In past research, for example, load voltage stabilization is achieved by using ON/OFF control^{(30)–(31)}; however, this introduces severe transients during the switching from ON state to OFF state, which put severe stress on the devices and can possibly cause false triggering and consequently control failure. In this view, the voltage stabilization of constant power load should be performed smoothly and with no communication signal in order to avoid control faults due to delay. Therefore, this paper proposes a secondary-side-only control for a single AC/DC converter based on symmetric phase shift. Given that only one converter exists in the secondary side, this approach does not consider the cascaded topology which adds another converter and complicates the system. The target application for this system is a constant power load such as a motor for EVs, which usually works with powers on the order of kilowatts and requires high voltages. Consequently, in case of the target application, the full-bridge topology is the most convenient because the system becomes very simple and symmetric. The control concept and the stability analysis are provided, and its effectiveness is verified by experiments both in static and dynamic conditions. This paper is organized into seven sections. Section 2 introduces the case of study and describes the power characteristics of WPT. Section 3 explains the proposed control concept and Section 4 presents the experimental results. Section 5 shows the results in case of variation of mutual inductance and Section 6 provides an evaluation on the efficiency. Finally, Section 6 draws the conclusions and indicates the future works.

2. Case of Study

This study focuses on the secondary side of a WPT system with SS compensation, as shown in the equivalent circuit of Fig. 1. It includes one converter per side, which is a configuration allowing bidirectional power flow. In the primary side there is an inverter used only to produce the high frequency square wave, while in the secondary side there are a full bridge active rectifier and the CPL such as a motor driven by a three-phase inverter as in⁽³⁰⁾. Both the inverter and the rectifier have H-bridge topology with four power MOSFETs. The operation between primary side and secondary is completely independent as it is performed from two different driver ports. The power transmitted to the secondary side is equal to:

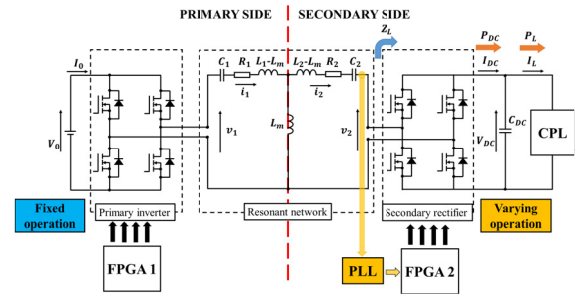


Fig. 1. Reference equivalent circuit

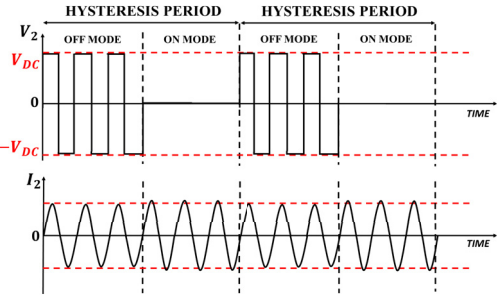


Fig. 2. Operation waveforms of ON/OFF control as described in⁽³⁰⁾

$$P_{DC} = \frac{(\omega L_m)^2 Z_L}{\{R_1(R_2 + Z_L) + (\omega L_m)^2\}^2} V_1^2 \dots \dots \dots (1)$$

with V_1 as RMS value of primary side voltage and Z_L as load input impedance. Considering a system in resonance, the fundamental waveforms of AC voltage v_2 and AC current i_2 are sinusoidal waves which are in phase, and the input impedance is regarded as a pure resistance. The power in (1) is thus real power. Furthermore, in condition of resonance it is allowed to approximate the AC voltages (v_1 and v_2) and currents (i_1 and i_2) by considering only the fundamental wave components. Past research almost never considered the CPL as a load without the battery component. If there is no battery, no voltage stabilization effect is available in case of control failure. In battery chargers CPL characteristics can be achieved, but this issue does not occur. Moreover if there is no battery in the CPL, the DC capacitor has a noticeable effect on the behaviour and is an important factor to be considered when designing the control. Supplying the battery but not the motor means that the power must reach the motor from the battery again with losses on the way. From a pure efficiency point of view, this is not an optimal solution, although useful. In⁽³⁰⁾ and⁽³¹⁾, the voltage stabilization by the secondary side is performed by using the ON/OFF control as an hysteresis to regulate the input voltage RMS value V_2 , as shown in Fig. 2, and keep the desired value of secondary DC voltage V_{DC} . The problem of this modulation method is that, when the switching from ON to OFF occurs, there are big current transients that are harmful to converters. Therefore, in this paper, another type of regulation is proposed. The control is applied to the secondary side full active rectifier and uses the combination of synchronous rectification (SR) and symmetric phase shift. The controller is a simple proportional-integral (PI) feedback. Instead of proportional-integral-derivative (PID) control, a PI was used because the transfer function of the plant is of the first order, as will be

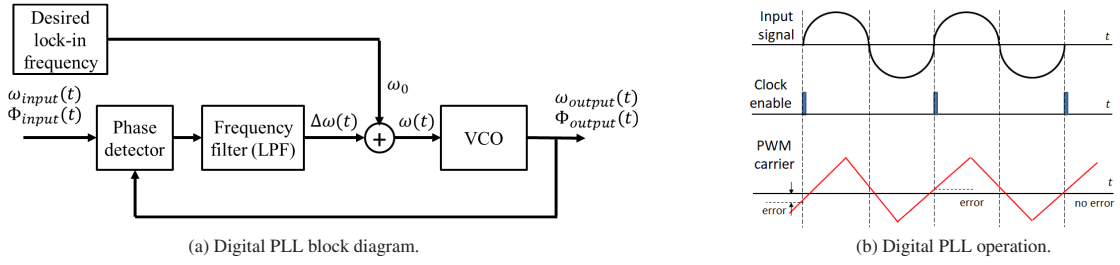


Fig. 3. Digital PLL

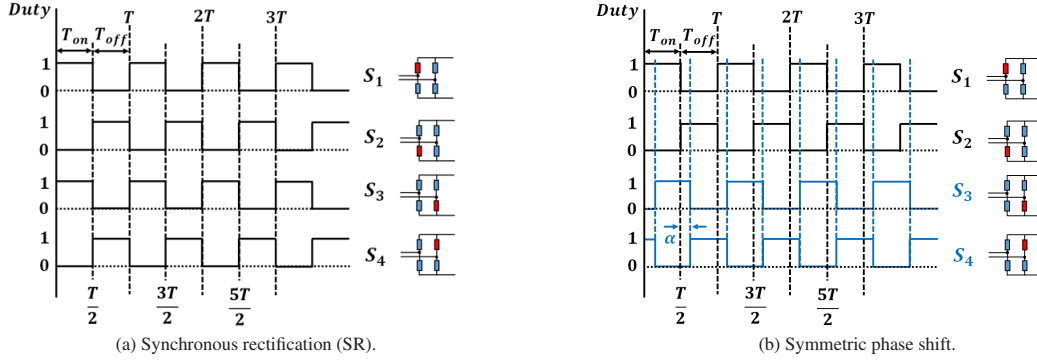


Fig. 4. Duty pattern of SR and symmetric phase shift

described in subsection 2.3, and consequently a PI controller is enough to meet the requirements. Furthermore, a PI controller is easier to design and tune. In order to design the controller, however, it is first necessary to analyze the load plant in case of CPL and counteract the slow pole typical of CPL.

2.1 Symmetric Phase Shift by use of Digital PLL with FPGA Since the primary side is considered fixed, the control must be performed on the secondary side rectifier. In other words, the rectifier has to be equipped with MOSFETs, which are controllable and are more suited to high frequency operation rather than IGBTs. The load is a CPL, which requires voltage stabilization because its open loop plant is unstable. In particular, having only one rectifier on the secondary side, the control must perform at the same time synchronization to the primary side and load voltage stabilization without recurring to discontinuous operation or primary side regulation. Hence, in this paper the chosen control method is symmetric phase shift as in Fig. 4(b).

In order to perform SR, it is necessary to adopt an analog polarity circuit or implement a digital phase locked loop (PLL). Given the high frequency environment, an analog circuit is preferable; however, it is an additional circuitry that occupies space. Therefore, coping with the constraint condition, the only solution is to use a digital phase locked loop (PLL). In this sense, a high performance control board with fast sampling time and calculation time is necessary: in other words, a field programmable gate array (FPGA) is mandatory. The digital PLL control block is shown in Fig. 3(a). It comprises of three main elements: a phase detector, a low-pass filter and a voltage controlled oscillator (VCO). The phase detector compares the phase for every sampling period and generates an error signal proportional to the phase difference between input and output. It is generally done by multiplying the two signals, then the output will have twice the input frequency and be proportional to the cosine of the

phase difference. The cut-off frequency of the low pass error filter is selected so that all the harmonic components at integer multiples of the excitation frequency are properly attenuated, leaving out only the low frequency components associated to the phase shift. The VCO is a linear time-invariant system whose oscillation frequency is determined by the input voltage. The loop gain must be high to reduce phase errors. In WPT systems, the variable fed to PLL is generally AC current; in this case of study, too, the input of the loop is i_2 , measured with a high bandwidth current sensor. The implementation concept is simple, as shown in Fig. 3(b). At every clock enable, decided by the sampling frequency of the board and set by the user, the phase error between the i_2 and the PWM carrier used in firing the devices of the secondary side AC/DC converter is calculated. The error is then fed to a PI feedback controller, whose task is to correct the incremental frequency of the PWM carrier. The reference signal and the feedback signal are periodic and the average value over the common period of their product only depends on the phase shift between the reference and the fundamental harmonic of the feedback. That means that even if the feedback signal contains harmonics and/or the measurement has an offset, performance of the phase-tracking algorithm will not be affected. Also, the PLL will be in equilibrium when the fundamental component of the feedback signal is 90 degrees shifted with respect to the reference signal. Of course, if the error is zero, then the variable and the PWM carrier are in phase and the phase is locked. When this situation happens, it is possible to activate the control for SR without fear of waves with different phase between primary side and secondary side.

With normal SR of Fig. 4(a), the output voltage v_{out} of the converter using SR is a square wave and the converter duty cycle is fixed at 0.5 because of the positive and negative halfwave. However, by modifying the parameter t_α , v_2 becomes the three-level waveform represented in Fig. 5 and

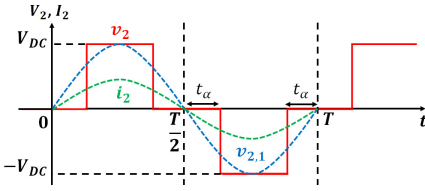


Fig. 5. Three-level voltage waveform of v_2 as in the proposed control

symmetric phase shift operation is achieved. In so doing, the amplitude of the fundamental waveform component of the output voltage v_{out} , which depends on V_{in} , changes accordingly to t_α as expressed in the following formula:

$$v_1 = \frac{2\sqrt{2}}{\pi} V_0 \cos\left(2\pi \frac{t_\alpha}{T}\right) \dots \dots \dots (2)$$

with T as the period of the waveform. This relationship can be applied to the secondary side active rectifier. The equation will be as follows:

$$v_2 = \frac{2\sqrt{2}}{\pi} V_{DC} \cos\left(2\pi \frac{t_\alpha}{T}\right) \dots \dots \dots (3)$$

with V_{DC} as the secondary DC voltage. For square wave operation, t_α is equal to zero. The duty cycle in case of symmetric phase shift is still equal to 0.5, but the phase shift ratio is different. It can be expressed by:

$$d_{cr} = \frac{t_\alpha}{T} \dots \dots \dots (4)$$

By changing the RMS value of v_{out} , the RMS value of the converted DC current I_{DC} varies as well. In fact, during phase shifting, the RMS value of output current $I_{DC,PS}$ will be only a fraction of its square wave correspondent $I_{DC,SW}$. Their slightly approximated relationship is given by:

$$I_{DC,PS} \approx I_{DC,SW} \cos(2\pi d_{cr}) \dots \dots \dots (5)$$

It is then possible to identify the conversion ratio α , given by:

$$\alpha = \cos(2\pi d_{cr}) \dots \dots \dots (6)$$

As a case of application, the case of study of the secondary side active rectifier and its output current is considered. In normal square wave operation, the RMS value of secondary current I_2 is expressed as:

$$I_2 = \frac{\omega L_m V_1 - R_1 V_2}{R_1 R_2 + (\omega L_m)^2} \dots \dots \dots (7)$$

Hence, $I_{DC,SW}$ is given by (neglecting the internal diodes' forward voltage drop):

$$I_{DC,SW} \approx \frac{2\sqrt{2}}{\pi} I_2 \dots \dots \dots (8)$$

On the other hand, in case of a phase shifting operation, (8) becomes the following expression based on (5):

$$I_{DC,PS} = I_{DC}(\alpha) = \frac{2\sqrt{2}}{\pi} \frac{\omega L_m V_1 - R_1 V_2 \alpha}{R_1 R_2 + (\omega L_m)^2} \alpha \dots \dots \dots (9)$$

The second term in the denominator ($R_1 V_2$) is much smaller than the other ($\omega L_m V_1$) and therefore can be ignored. By phase shifting, $I_{DC}(\alpha)$ is modified in such a way that stabilization is ensured.

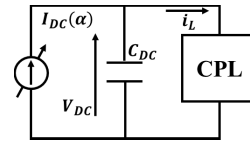


Fig. 6. Equivalent circuit of CPL

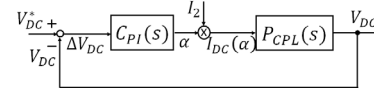


Fig. 7. Proposed controller

2.2 Controller Design for CPL The equivalent circuit for the constant power load considered in this circuit is shown in Fig. 6. Its characteristic equations is as following:

$$i_L = I_{DC}(\alpha) - C_{DC} \frac{dV_{DC}}{dt} \dots \dots \dots (10)$$

$$|Z_L| = \frac{V_{DC}^2}{P_L}, \quad P_L = V_{DC} i_L$$

where C_{DC} is the DC smoothing capacitor. These characteristic equations are non-linear and therefore need to be linearized. The linearization is performed by setting an equilibrium point at voltage V_{eq} and current I_{eq} and considering the variation around it as following:

$$V_{DC} = V_{eq} + \Delta V_{DC} \dots \dots \dots (11)$$

$$I_{DC}(\alpha) = I_{eq} + \Delta I_{DC}(\alpha) \dots \dots \dots (12)$$

Here, the voltage V_{eq} and current I_{eq} are the load voltage and current at the operation point. Hence, the following approximated open loop transfer function is obtained:

$$P_{CPL}(s) = \frac{\Delta V_{DC}(s)}{\Delta I_{DC}(\alpha)(s)} \dots \dots \dots (13)$$

$$\approx \frac{1}{C_{DC} \left(s - \frac{P_L}{C_{DC} V_{eq}^2} \right)}$$

In (14), it is clear that the pole resides in the right half plane. More in detail, it depends on load power P_L , DC voltage V_{DC} and smoothing DC capacitor C_{DC} . For bigger P_L , smaller V_{DC} and smaller C_{DC} , the poles are faster. Past research on CPL voltage stabilization is abundant in the case of power distribution, but in case of WPT it has rarely if ever been performed. In this paper, the stabilization of V_{DC} is performed by a high bandwidth PI controller as shown in Fig. 7. Thus, the controller regulates the value of v_2 by adapting t_α . The controller gains are chosen by pole placement method. From the Routh stability criterion the following formulations must be satisfied in order to maintain stability:

$$k_p \geq \frac{P_L}{V_{eq}^2} \dots \dots \dots (14)$$

$$k_I \geq 0 \dots \dots \dots (15)$$

Then, choosing the damping factor ψ equal to one, the gains can be chosen according to:

$$k_p = \frac{2mZ_L^* C_{DC} - 1}{Z_L^*} \dots \dots \dots (16)$$

$$k_I = m^2 C_{DC} \dots \dots \dots (17)$$

where m is the pole in closed loop. In (16), Z_L^* is determined by the desired operating voltage V_{DC}^* and the load power P_L as follows:

$$Z_L^* = \frac{V_{DC}^{*2}}{P_L} \dots \dots \dots (18)$$

It is clear that the proportional gain is variable. In any case, m must be chosen high enough to avoid frequency bifurcation and other phenomena occurring at slow pole position. It is obvious that by using a two degree of freedom PI control, which include the feedforward part, it is easier to design the controller by choosing a lower frequency during pole placement. However, in this research, the basic case is introduced, not to mention that the feedback controller design is the very same.

3. Experimental Results

3.1 Stability Conditions Depending on Operation Point Parameters The experimental setup is shown in Fig. 8 and the circuit parameters are reported Table 1. As in Fig. 1, a FPGA is used to control independently both the converters in the systems. The primary side v_1 and mutual inductance L_m are fixed, therefore the RMS value of i_2 is fixed, too. In the experiments, the stability of the proposed control is verified by changing step-wise the voltage reference V_{DC}^* . The results are presented in Fig. 9, Fig. 10 and Fig. 11.

In Fig. 9, the three-level operation explained in Fig. 5 is confirmed. The little surges on v_2 depend on the fact that a single FPGA is used to control at the same time both converters in primary and secondary side. It is noticed that the noise is generated at the switching of the primary side, therefore it must have found a path through the FPGA since the resonance network in case of magnetic resonance coupling has bandpass filter properties. Nevertheless, the control effectiveness is not affected by this issue, as the voltage is stable and the value of V_2 has never been a problem either in steady state or during transient.

In Fig. 10, the change in V_{DC} (blue line) and i_L (red line) is shown; on the other hand, in Fig. 11 the change in α is shown. Moreover, in Fig. 10(a) and Fig. 11(a) the power P_L is 1 W, while in the other case P_L is 1.5 W. Furthermore, in Fig. 10(a) and Fig. 11(a) the V_{DC}^* changes from 3 V to 4 V, while in Fig. 10(b) and Fig. 11(b) the V_{DC}^* varies from 3.5 V to 4 V. As it can be seen, in Fig. 10(a) and Fig. 10(b) the voltage stability is maintained.

In Fig. 11 the variation of α is shown. The variation of α happens in two stages. At $t = 0$, the voltage reference is changed. Since the new reference is higher, it is necessary to match it. During reference matching phase, α becomes one to charge the DC capacitor and match the new reference voltage with full synchronous rectification. When the voltage value is close to V_{DC}^* , the stabilization phase begins. Here, the control lowers α down to a different value, related to the required AC/DC converter output current $I_{DC}(\alpha)$. This new value is the stabilized value, which must be lower than one otherwise the closed loop function will behave just like the open loop function. Thus, by looking at the initial value and the final value of α reported for each case in Fig. 11, it is verified that in Fig. 11(a) the final value is 0.3. Similarly, in the

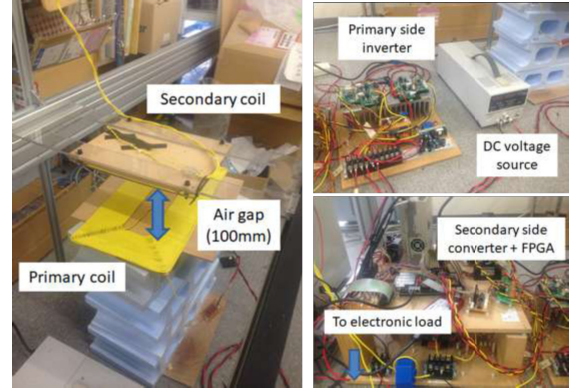


Fig. 8. Experimental setup

Table 1. System parameters for CPL experiment

Parameter	Value
Primary side DC voltage source V_0	10 V
Primary side coil resistance R_1	1.83 Ω
Secondary side coil resistance R_2	1.683 Ω
Primary side coil inductance L_1	417.8 μH
Secondary side coil inductance L_2	208.3 μH
Primary side coil capacitance C_1	6.03 nF
Secondary side coil capacitance C_2	12.15 nF
Operation frequency f	100 kHz
Mutual inductance L_m (best alignment)	37.9 μH
Coil gap (best alignment)	100 mm
Smoothing capacitor C_{DC}	1000 μF

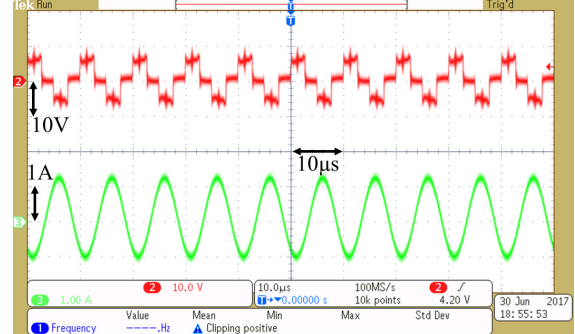


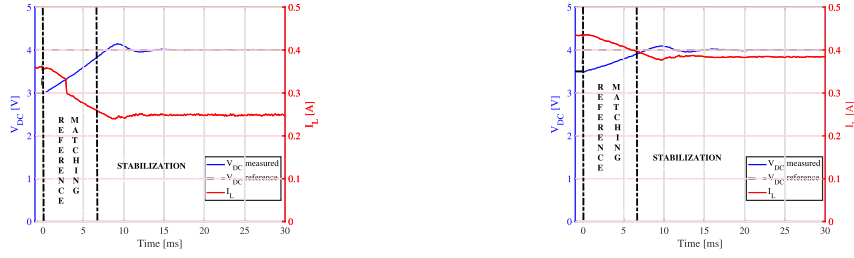
Fig. 9. AC variables (red:voltage v_2 ; green:current i_2) with $V_{DC} = 4$ V, $P_L = 1$ W

case of Fig. 11(b) the final value is 0.5. As expected, both are different from one and result in stability. Thus, from these experiments it is verified that stability is achieved.

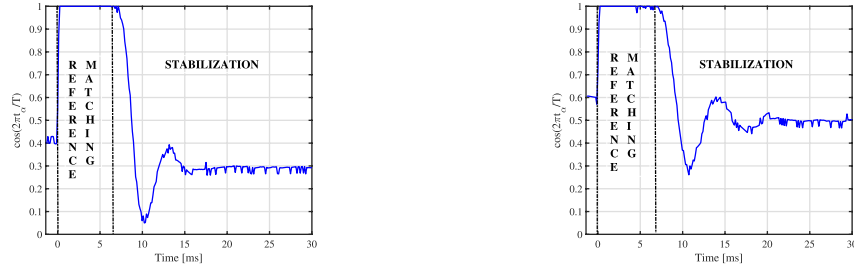
In the previous sections, the necessity of a controller for stabilizing the load voltage has been made clear. The controller design presented grants stability in the wide operation area because of the adaptive gains calculated from pole placement. However, there are some physical limitation deriving from the system parameters that are unavoidable (e.g. conversion ratio of a converter can not be higher than one, $\alpha \leq 1$). This applies in the case of wireless power transfer systems for CPL. In fact for a determined load power, by considering (10), in steady state the maximum current $I_{DC}(\alpha)$ is given by:

$$I_{DC}(\alpha)|_{\alpha=1} = \frac{2\sqrt{2}}{\pi} \frac{\omega L_m V_1 - R_1 V_2}{R_1 R_2 + (\omega L_m)^2} \dots \dots \dots (19)$$

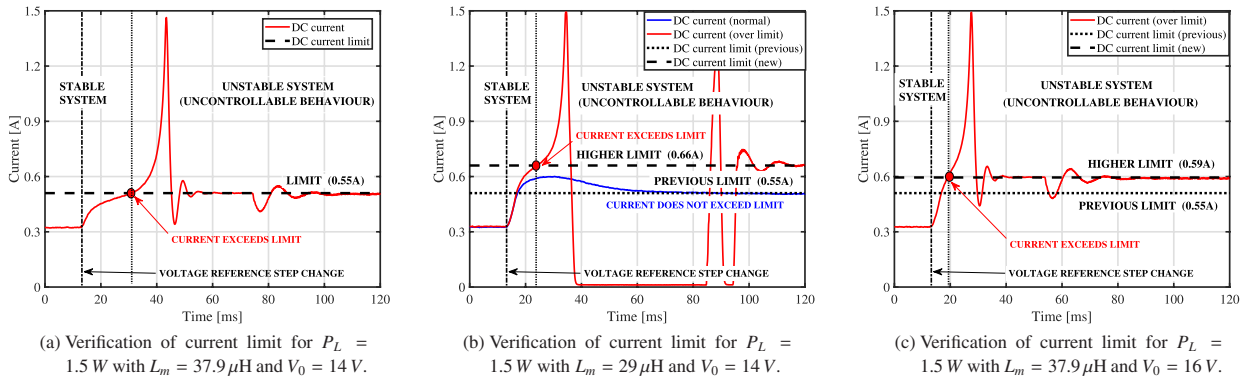
and therefore, because of (10), also the voltage V_{DC} is



(a) Reference V_{DC}^* from 3 V to 4 V, power $P_L = 1$ W. (b) Reference V_{DC}^* from 3.5 V to 4 V, power $P_L = 1.5$ W.
Fig. 10. Experimental results of proposed control: profile of V_{DC} and i_L when the voltage reference is changed



(a) Reference V_{DC}^* from 3 V to 4 V, power $P_L = 1$ W. (b) Reference V_{DC}^* from 3.5 V to 4 V, power $P_L = 1.5$ W.
Fig. 11. Experimental results of proposed control: profile of secondary side conversion ratio α when the voltage reference is changed



(a) Verification of current limit for $P_L = 1.5$ W with $L_m = 37.9 \mu\text{H}$ and $V_0 = 14$ V. (b) Verification of current limit for $P_L = 1.5$ W with $L_m = 29 \mu\text{H}$ and $V_0 = 14$ V. (c) Verification of current limit for $P_L = 1.5$ W with $L_m = 37.9 \mu\text{H}$ and $V_0 = 16$ V.
Fig. 12. Verification of current $I_{DC}(\alpha)$ limit

limited. Its value is expressed by:

$$V_{DC}(\alpha)|_{\alpha=1} = \frac{P_L}{I_{DC}(\alpha)|_{\alpha=1}} \dots \dots \dots (20)$$

which is the minimum value possible for a given load power. In this case, a secondary converter for physical decoupling and further control is not available, therefore I_{DC} and V_{DC} will not undergo further conversions. Thus, (19) and (20) hold for the load parameters i_L and v_L as well.

This can be verified with an experiment by showing how the current limit changes by varying the mutual inductance L_m and the DC source voltage V_0 . The experiments are shown in Fig. 12. The experiment is performed by purposely changing the voltage reference V_{DC}^* to a value lower than the one calculated by using (20) in order to increase the load current as the load is CPL. At $t = 13$ ms, the reference change command is given and the behaviour of the current $I_{DC}(\alpha)$ is observed. As a starting condition, the parameters adopted are the same as Table 1 and the reference power is 1.5 W.

In Fig. 12(a) the current limit calculated for the abovementioned conditions is 0.55 A, expressed by the dashed line. In other words that 0.55 A is the current flowing in the secondary side when the secondary side conversion ratio α is

equal to one, which is the same of open loop condition. After the change in voltage reference, the current runs away at the moment it surpasses the limit and stops at 1.5 A because of the overcurrent protection. In the meantime, the voltage V_{DC} becomes nearly zero. After the current exceeds the limit of 0.55 A, the system behaviour is uncontrolled and therefore the waveforms have no particular meaning. Hence, it is confirmed that the stability is maintained as long as α is less than one. In order to show the importance of knowing the physical limits of voltage and current, two more experiments in different conditions are performed.

In Fig. 12(b), the mutual inductance L_m is decreased from $37.9 \mu\text{H}$ to $29 \mu\text{H}$, meaning that the coupling is more loose, the efficiency is lower and the available transmittable power is higher. All the other parameters are the same as the first case. In this case, it is expected that the current limit is higher: in fact, from the calculation it results that the limit is increased from 0.55 A to 0.66 A. By performing the very same change of V_{DC}^* as before, it is shown that the current (blue line) does not approach the limit because the maximum transient value has changed from 0.55 A (small dashed line) to 0.66 A (big dashed line); then, the stability is maintained. On the other hand, for a bigger change of V_{DC}^* , the current

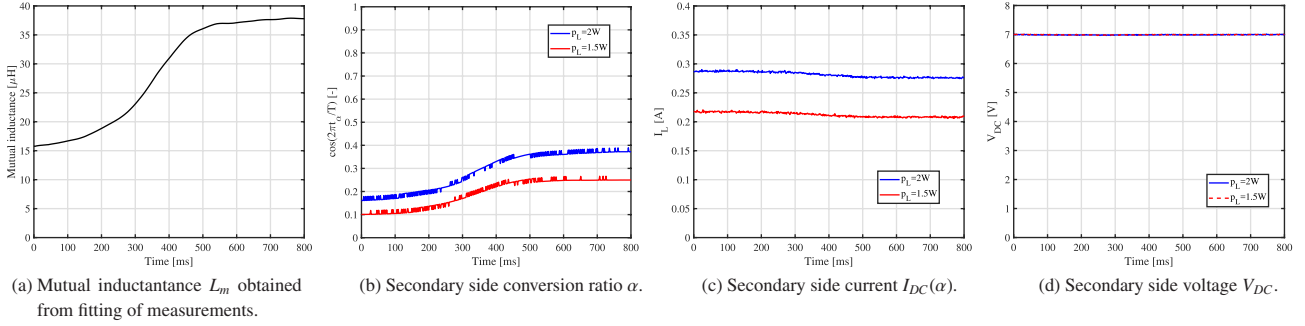


Fig. 13. Experimental results with mutual inductance variation

(red line) exceeds the limit and the stability is lost.

Finally, in Fig. 12(c), the DC voltage source V_0 is increased from 14 V to 16 V, meaning that the efficiency is slightly lower and the available transmittable power is higher. All the other parameters are the same as the first case. In this last case, too, the current limit becomes higher than the first case: the new limit value is 0.59 A (dashed line), while in the previous case it was 0.55 A. It is demonstrated once more that, when the voltage reference V_{DC}^* is big, the current $I_{DC}(\alpha)$ (red line) will run away at the moment the current limit is exceeded and the stability is lost because the α is trying to be bigger than one, which is impossible.

By viewing these results, the unavoidable limits of secondary-side-only control for voltage stabilization of CPL have been clarified. These limits can be modified by mutual inductance and primary source voltage. In particular, in Fig. 12(b) it is shown that the higher limit guarantees stability to the same step change that was unstable in Fig. 12(a). Coordination with the primary side, as in ⁽³⁰⁾, will allow to maintain stability by securing that the secondary DC current $I_{DC}(\alpha)$ never exceeds the limit; however, in case of dynamic WPT, it is very difficult to rely on the primary side. Consequently, secondary-side-only control is necessary.

4. Effect of Mutual Inductance Variation

Since one of WPT's main contribution is the enhanced mobility, it is expected that in target applications there are cases in which the coils are moving. In these condition of dynamic WPT, the mutual inductance L_m changes, and since the mutual inductance is relevant to many other parameters, it is necessary to ascertain that its change does not affects them negatively. Therefore, in the present investigation, it is necessary to verify that even with change in the mutual inductance the voltage V_{DC} does not change. The experiment results are reported in Fig. 13. In these experiments, the voltage reference V_{DC}^* is equal to 7 V, therefore it is expected that V_{DC} will be always 7 V notwithstanding any change in L_m .

In Fig. 13(a), the change of L_m is shown. In total, the mutual inductance increases from 16 μH to 37 μH in 700 milliseconds. As stated in a previous chapter, the mutual inductance can not be measured during the coil movement, therefore this graphic is obtained fitting the measured values at fixed operation points with some misalignment from the center, which is the best condition. In Fig. 13(b), the variation of the secondary side converter ratio α is reported for two different power levels: one is 2 W, the other one is 1.5 W. It is possible to see that α follows the same pattern as the mutual

inductance. This is because in WPT systems by magnetic resonant coupling with SS compensation, as the mutual inductance increases, the power delivered to the secondary side is reduced. Consequently, α correctly becomes large in order to let more current flow in the effort of keeping the voltage V_{DC} fixed to the reference. Even more obvious, for higher power α is higher because, at the same voltage level, the current must be higher.

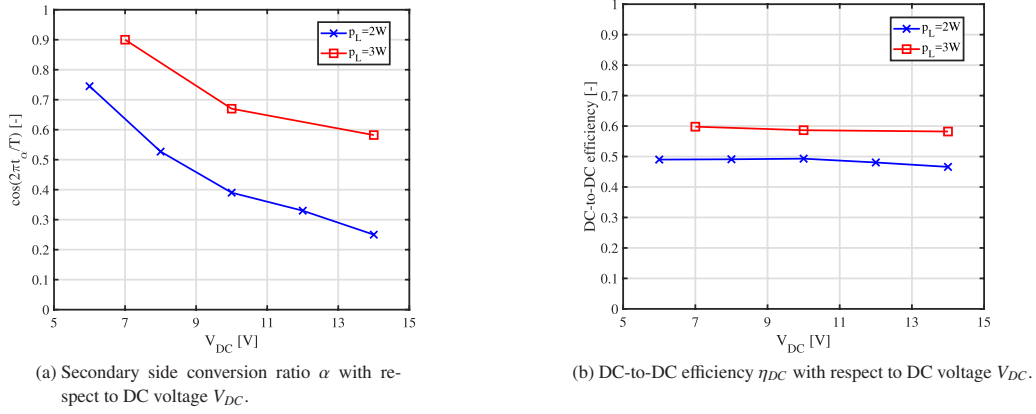
In Fig. 13(c), the current $I_{DC}(\alpha)$ is shown. Its value changes only slightly, becoming about 5% lower than the initial value. Finally, in Fig. 13(d), the voltage V_{DC} is shown. It is immediate to notice that the DC voltage V_{DC} is equal to 7 V, matching the reference and being unaffected from the change of L_m . The control is smooth and no transients are observed.

From these results it is apparent that the proposed controller copes well with changes of L_m and can be suitable for dynamic WPT applications.

5. DC-to-DC Efficiency Evaluation

By using symmetric phase shift the DC-to-DC efficiency η_{DC} is not very high because of the increased switching losses that are quite relevant in high frequency. These switching losses are higher in case of big voltage regulations and high power factor conditions. Unfortunately, this applies to the case of study under investigation because only one converter is available in the secondary side for the stabilization of V_{DC} . The maximum efficiency is achievable with synchronous rectification but, in the case of study, continuous synchronous rectification is an impossible operation mode because the CPL voltage cannot be stabilized. It is possible to use the ON/OFF modulation with short mode, however it will generate transients much bigger than the ones happening with the proposed phase shift voltage stabilization. Consequently, it is necessary to associate the secondary side conversion ratio α to the DC-to-DC efficiency η_{DC} and evaluate this relationship. The efficiency was not compared with other papers because the power level and circuit topology and consequently the type of control are different. The proposed control is only for voltage stabilization of CPLs. Efficiency control is not implemented in this paper, thus it would not be fair comparison since previous research proposed a system with optimized efficiency ⁽¹⁹⁾⁽³⁰⁾.

The experimental data is shown in Fig. 14. For different values of V_{DC} , at parity of other conditions, the values of α and η_{DC} are shown. For better evaluation, the results in the case of load power P_L equal to 2 W and P_L equal to 3 W are reported. The values of α and η_{DC} are the maximum


 Fig. 14. DC-to-DC efficiency evaluation by considering α

values achievable just before the unavoidable physical limitations related to the DC current $I_{DC}(\alpha)$. In Fig. 14(a), it is shown how changes α with different voltages. Of course, for lower values of V_{DC} , higher values of α will be obtained. Similarly, for higher power level, also α will be higher. In Fig. 14(b), the DC-to-DC efficiency η_{DC} is plotted with different voltage condition. Interestingly, the value of the conversion ratio α does not almost affect the efficiency, even for different values of DC voltage V_{DC} . It is however noted that, for higher load power P_L , the DC-to-DC efficiency is consequently higher. Therefore, it can be said that, while the proposed secondary-side-only voltage stabilization control with one converter achieves smooth transient, design simplicity and does not need communication, the efficiency is not very high. Efficiency can be increased by adding efficiency control⁽¹⁹⁾ to the stabilization or by optimizing the circuit parameters⁽³⁰⁾, thus operating in the high efficiency zone.

6. Conclusion

This paper proposes a control for voltage stabilization for WPT systems with CPL. The proposed control is performed only with a single full active rectifier on the secondary side, without communication to and regulation thereof of the primary side. The control consists in symmetric phase shift to change the amplitude of v_2 : this causes smoother transient when compared to stabilization by means of discontinuous operation. Furthermore, the controller is a simple PI feedback with high bandwidth applied to t_α . The controller design as well as the derivation of the controller gains is described.

Experimental results confirm the validity of the proposed method, covering different parameters variations in order to prove the stability of the load voltage. Given the lack of other converters for decoupling, there are intrinsic limits of stability depending on the DC source voltage and the mutual inductance. If the secondary current or the secondary voltage surpasses those limits, the stability cannot be maintained because of the unavoidable limitations of the secondary side conversion ratio α , which can not be higher than one.

Higher power experiments and efficiency improvement are the main direction of further investigation, as well as experiments with real motor loads.

Acknowledgment

This work is partly supported by JSPS KAKENHI grant number 15H02232 and number 17H04915 and the

JST-CREST grant number JPMJCR15K3. Moreover, the authors would like to express their deepest gratitude to Dr. Giuseppe Guidi for the precious discussions about the FPGA operation and settings.

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